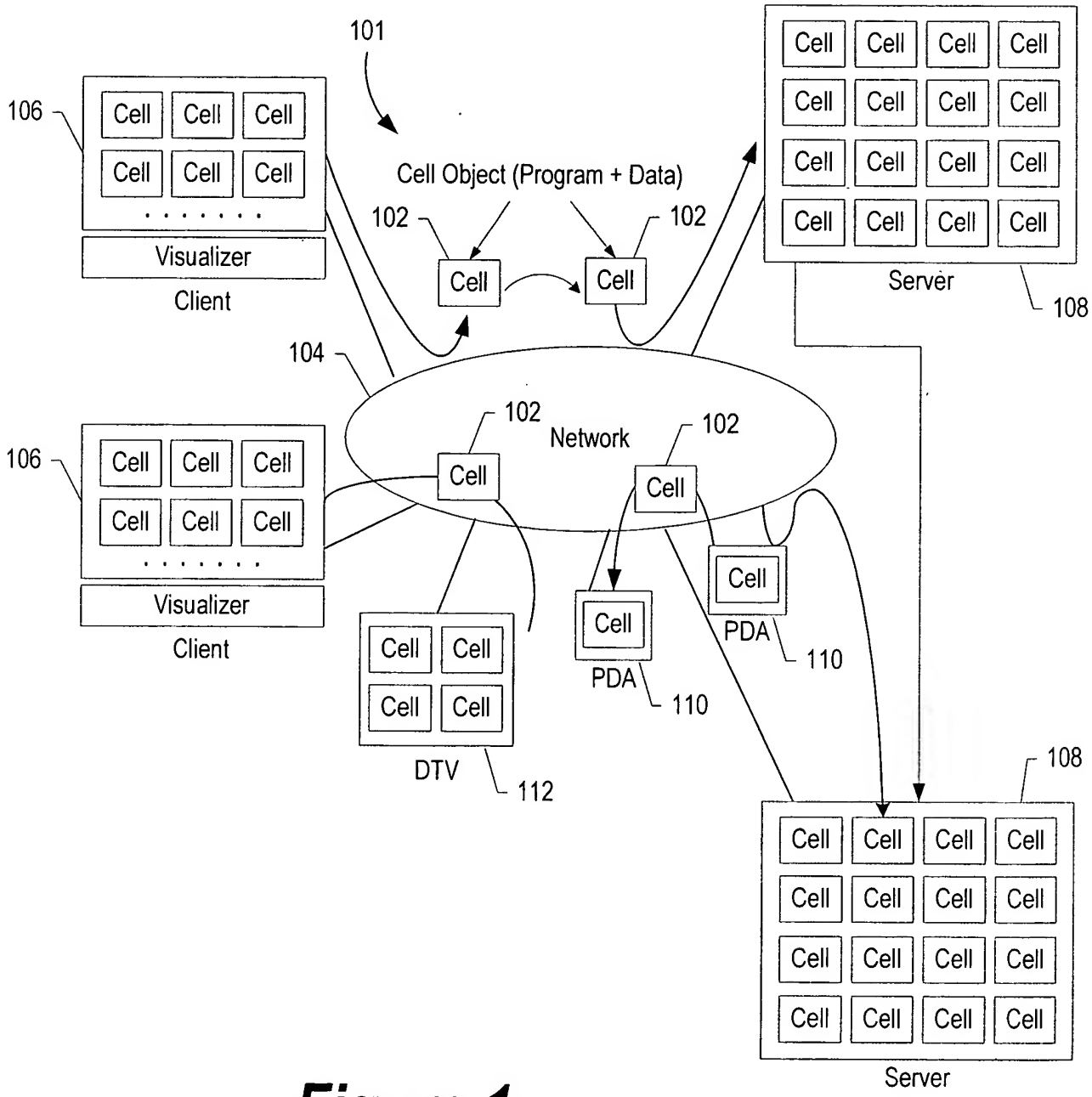
101
Cell Object (Program + Data)
102
102
Cell
Cell
106
Cell Cell Cell
Cell Cell Cell
Visualizer
Client
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Server
108
104
Network
102
102
Cell
Cell
106
Cell Cell Cell
Cell Cell Cell
Visualizer
Client
Cell
PDA
110
Cell
PDA
110
Cell Cell
Cell Cell
DTV
112
108
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Server

Figure 1

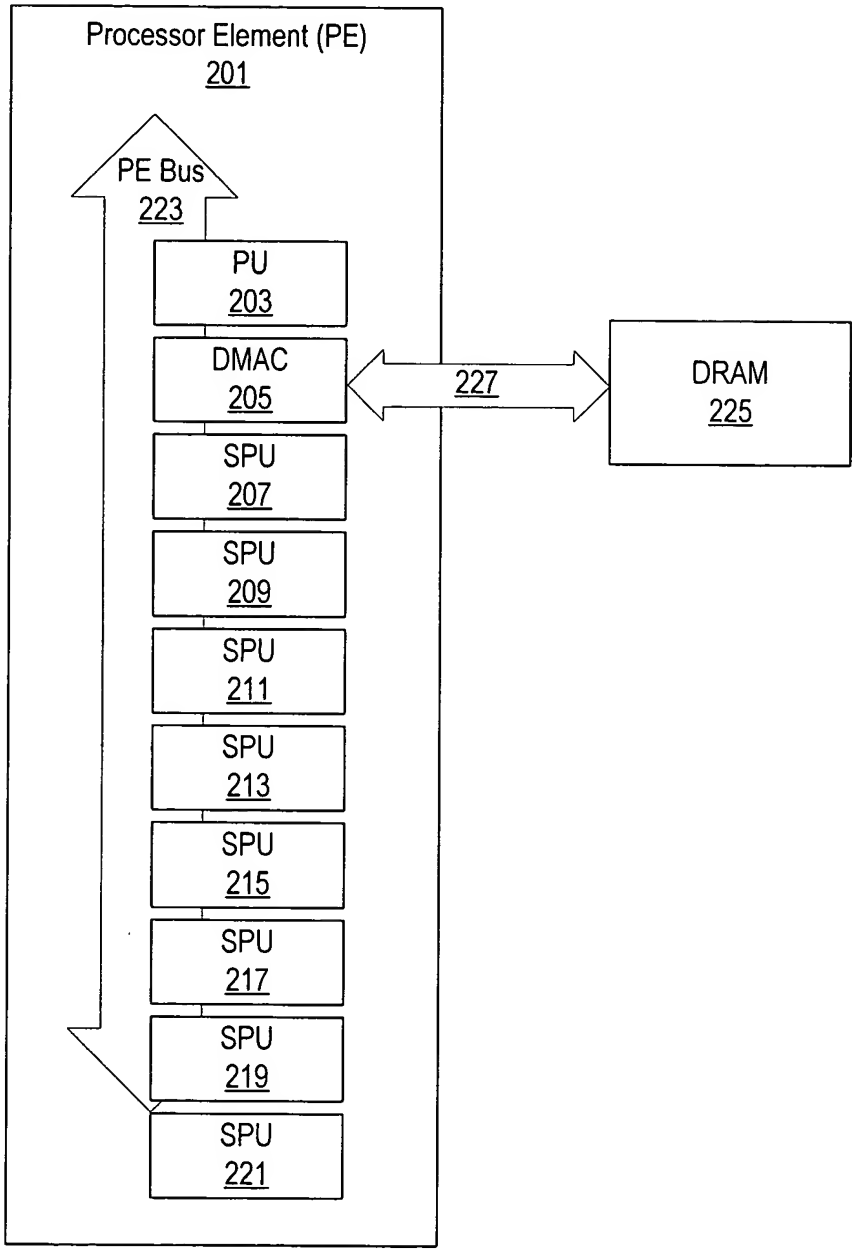
Processor Element (PE)
201
PE Bus
223
PU
203
DMAC
205
227
DRAM
225
SPU
207
SPU
209
SPU
211
SPU
213
SPU
215
SPU
217
SPU
219
SPU
221

Figure 2

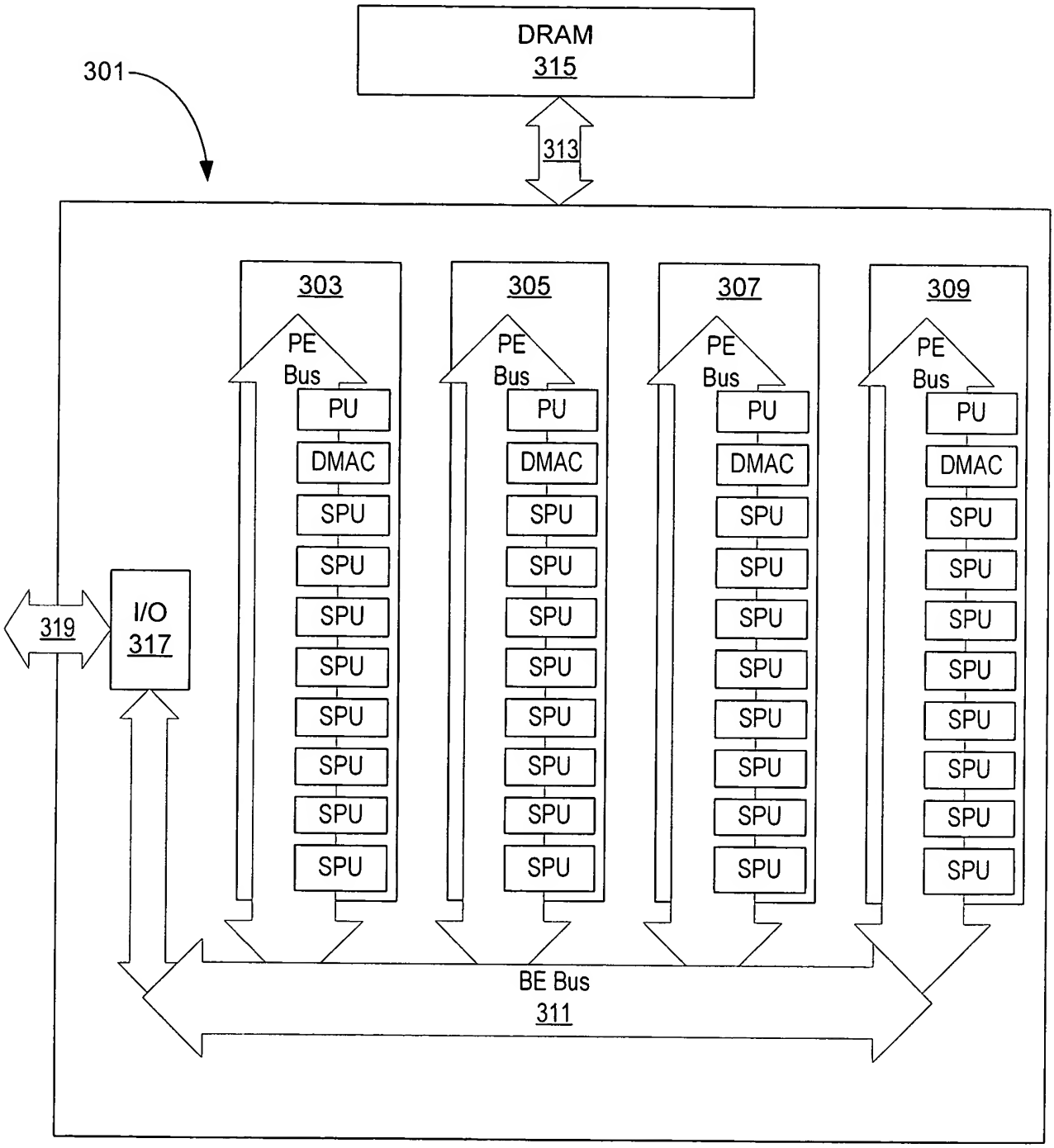
DRAM
315
301
313
303
305
307
309
PE
Bus
PU
DMAC
SPU
319
I/O
317
BE Bus
311

Figure 3

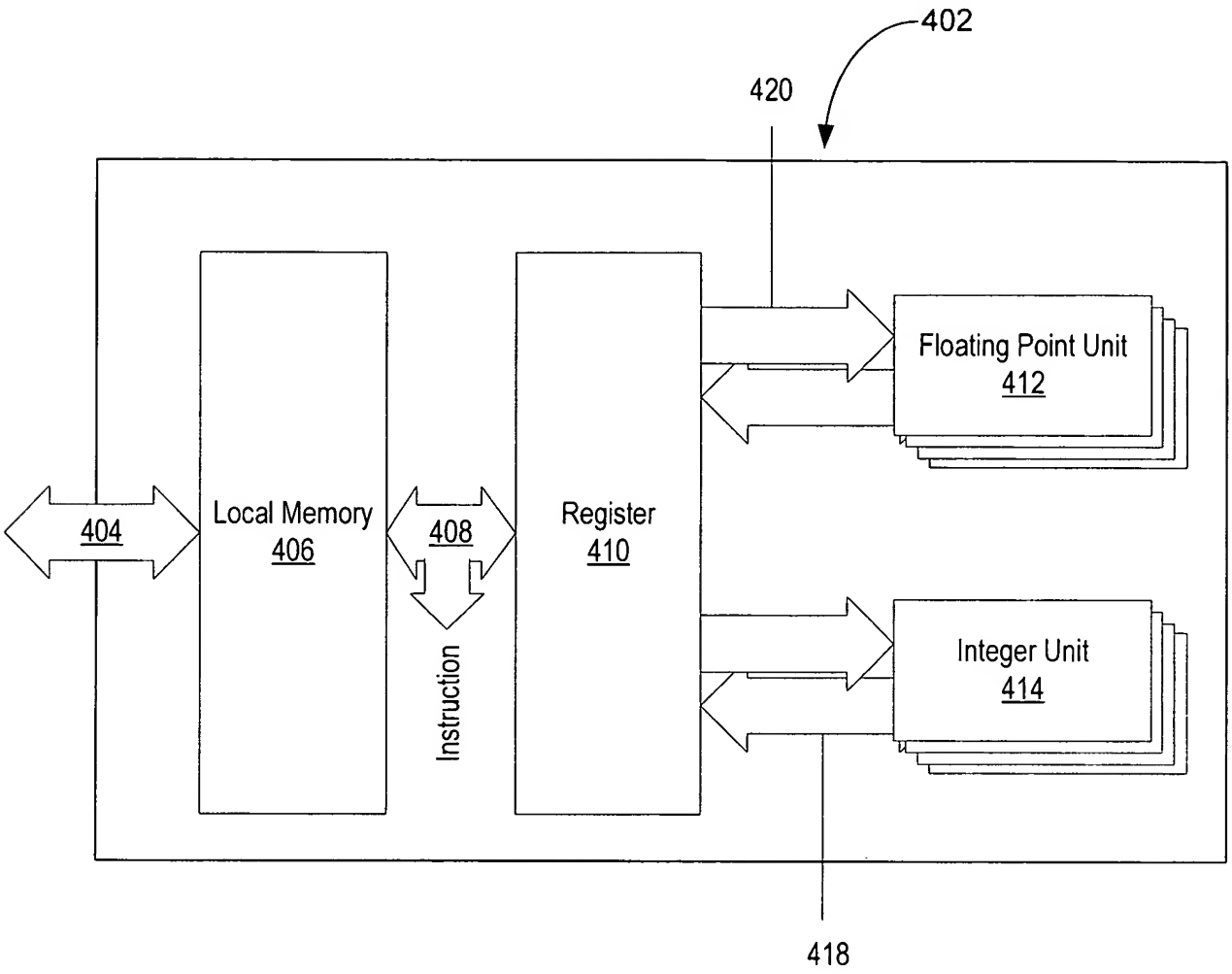
402
420
Floating Point Unit
412
Local Memory
406
404
408
Register
410
Instruction
Integer Unit
414
418

Figure 4

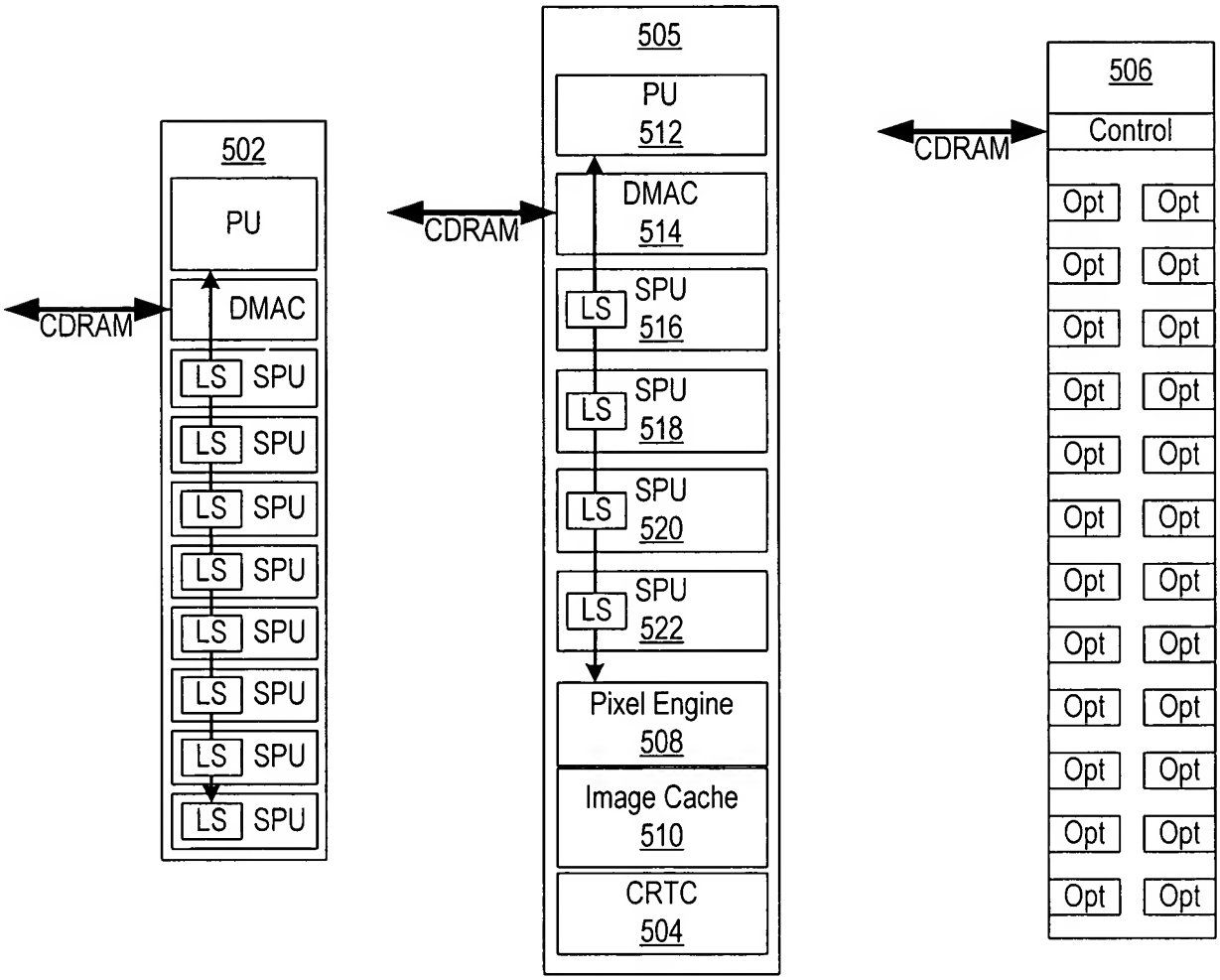
502
PU
DMAC
CDRAM
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
505
PU
512
DMAC
514
CDRAM
SPU
516
SPU
518
SPU
520
SPU
522
Pixel Engine
508
Image Cache
510
CRTC
504
506
Control
CDRAM
Opt

Figure 5

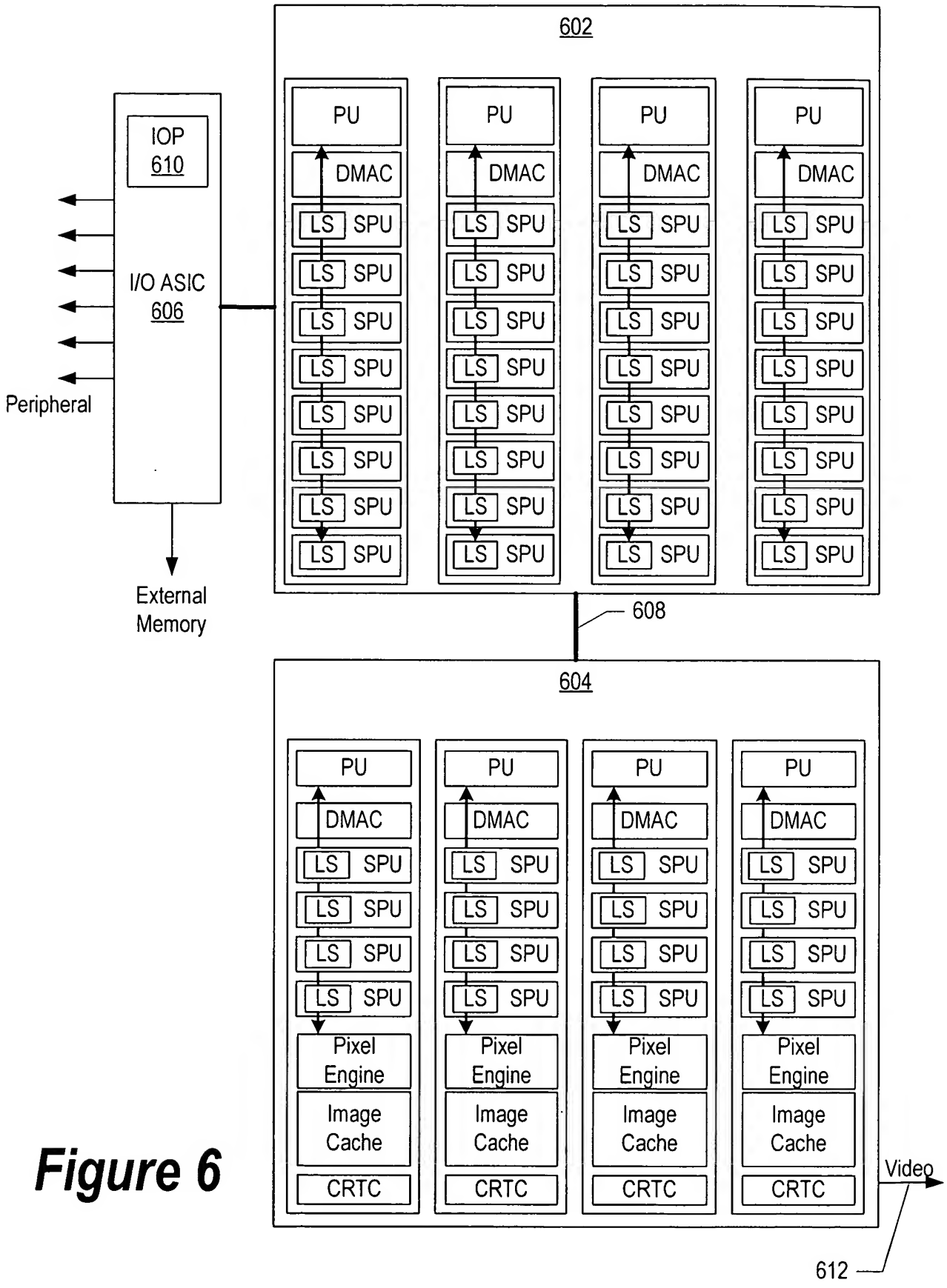
602
IOP
610
I/O ASIC
606
Peripheral
External
Memory
PU
DMAC
LS
SPU
608
604
Pixel
Engine
Image
Cache
CRTC
Video
612

Figure 6

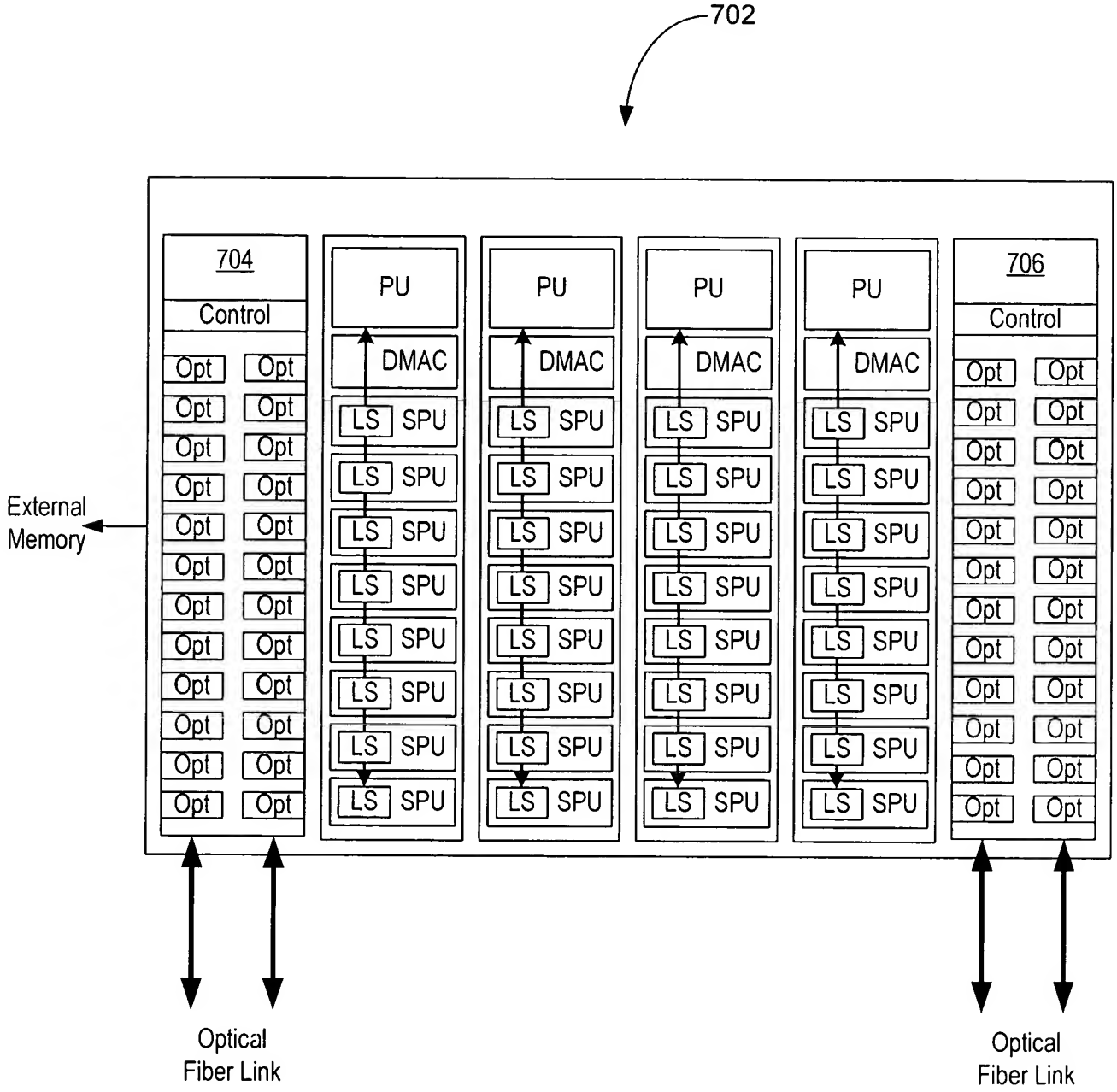
702
704
Control
Opt
PU
DMAC
LS
SPU
706
External Memory
Optical Fiber Link
Optical Fiber Link

Figure 7

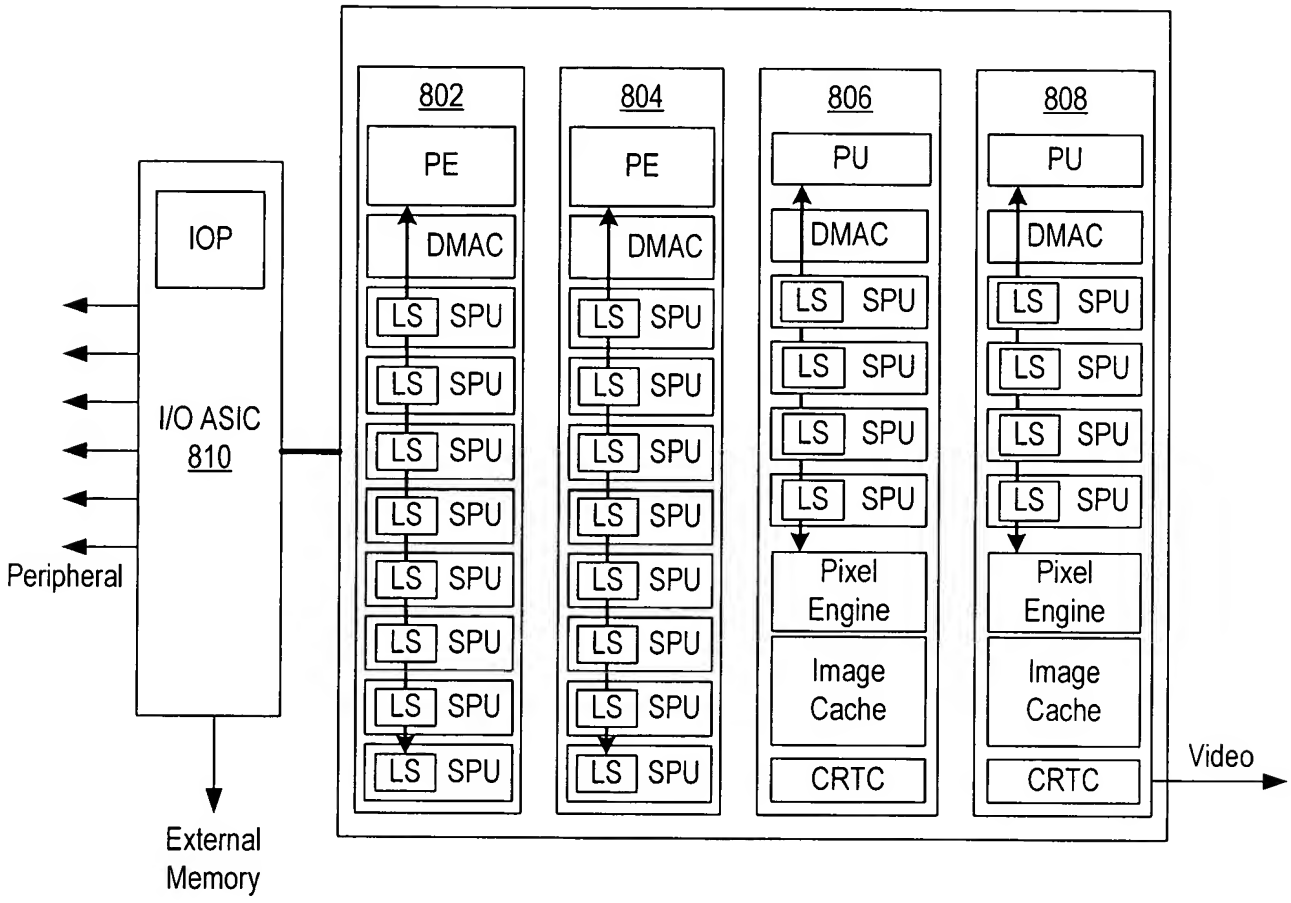
802
804
806
808
PE
PE
PU
PU
DMAC
DMAC
DMAC
DMAC
LS SPU
Pixel Engine
Image Cache
CRTC
IOP
I/O ASIC 810
Peripheral
External Memory
Video

Figure 8

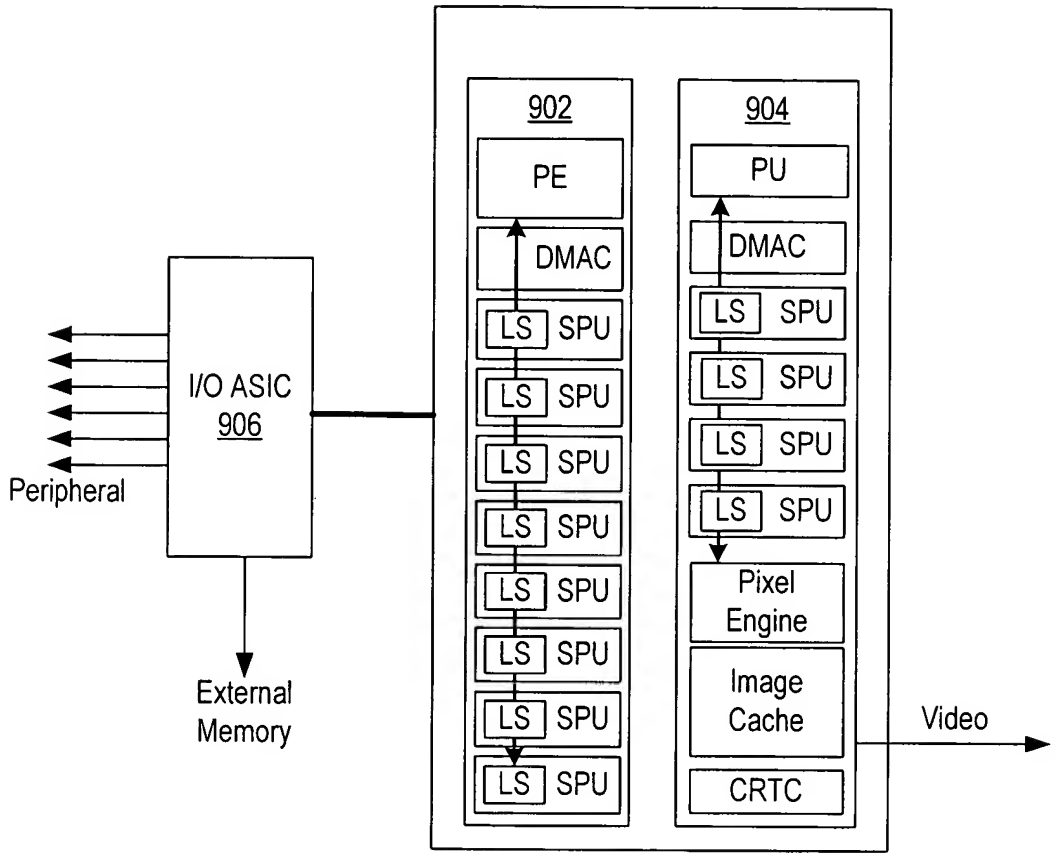
902
PE
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
904
PU
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
Pixel Engine
Image Cache
CRTC
Video
I/O ASIC 906
Peripheral
External Memory

Figure 9

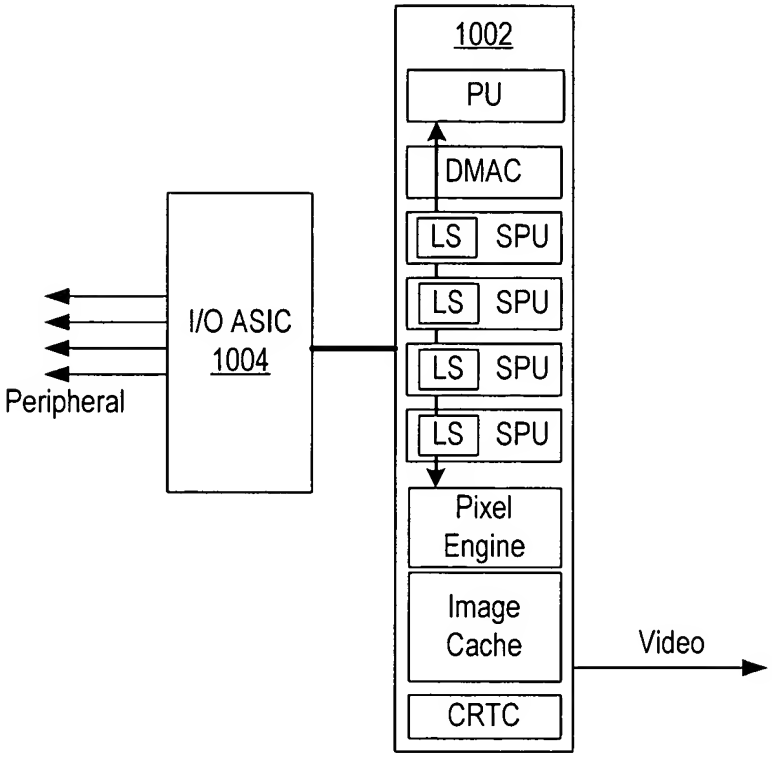
1002
PU
DMAC
LS
SPU
LS
SPU
LS
SPU
LS
SPU
Pixel Engine
Image Cache
CRTC
I/O ASIC
1004
Peripheral
Video

Figure 10

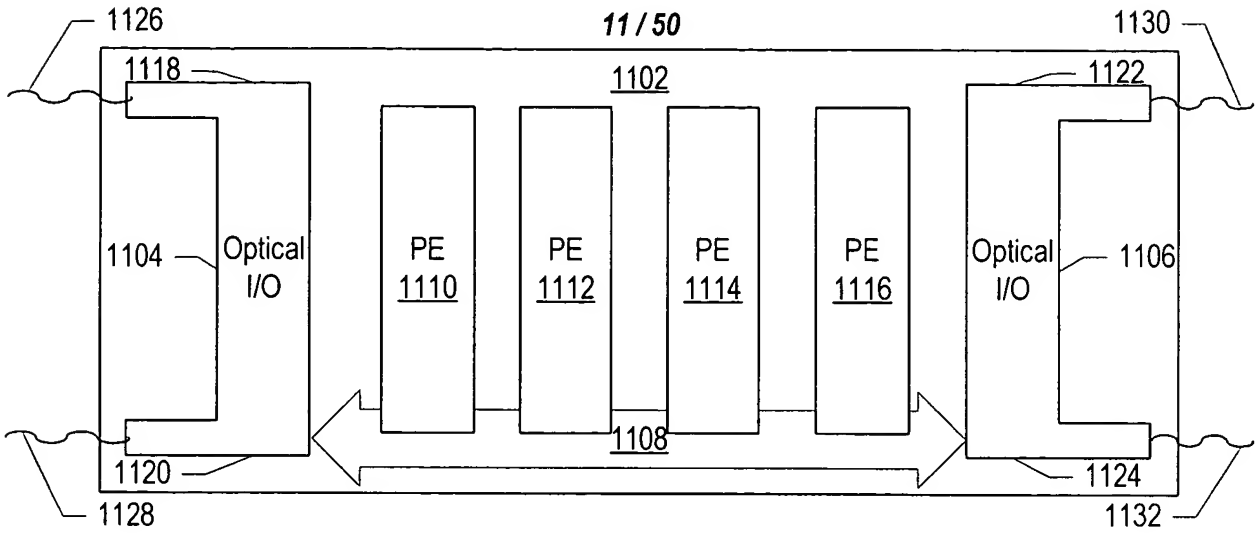

Figure 11A

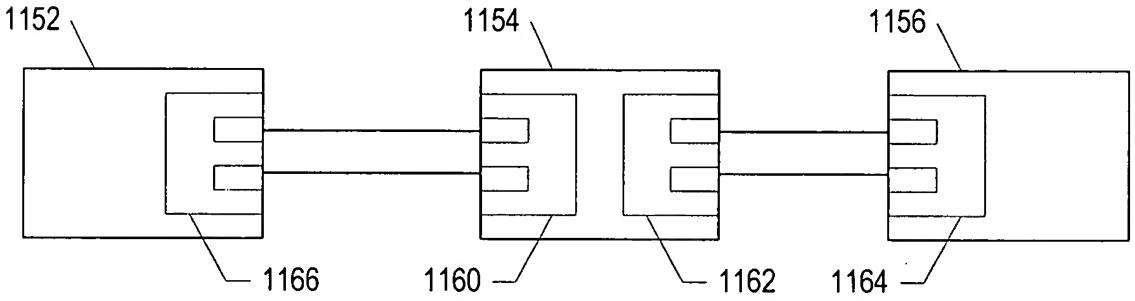

Figure 11B

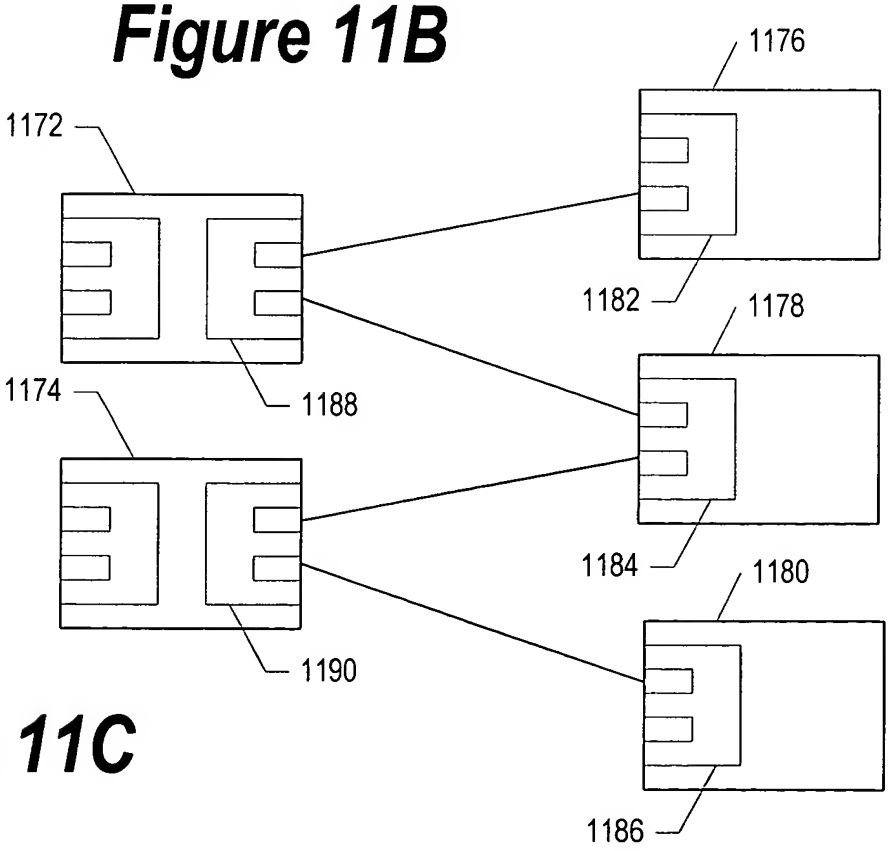

Figure 11C

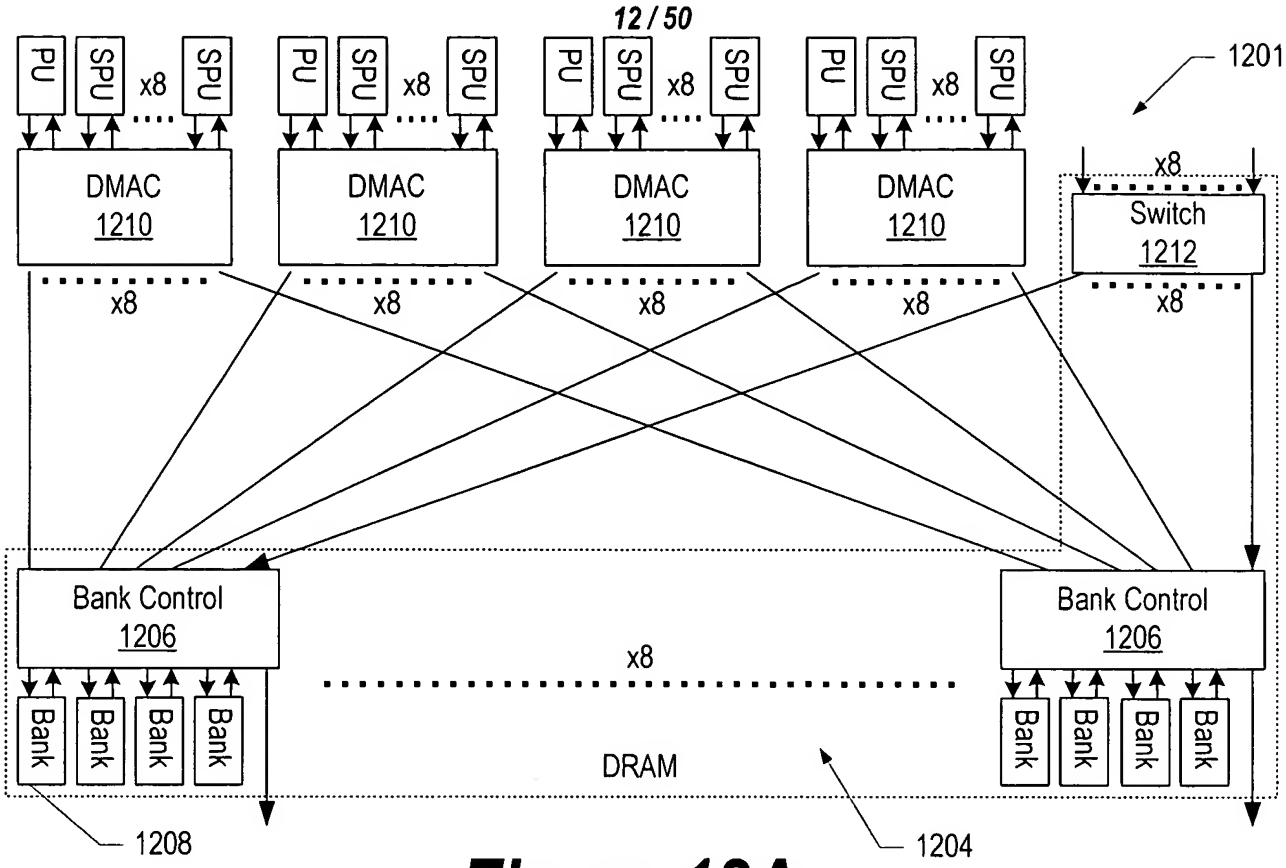

Figure 12A

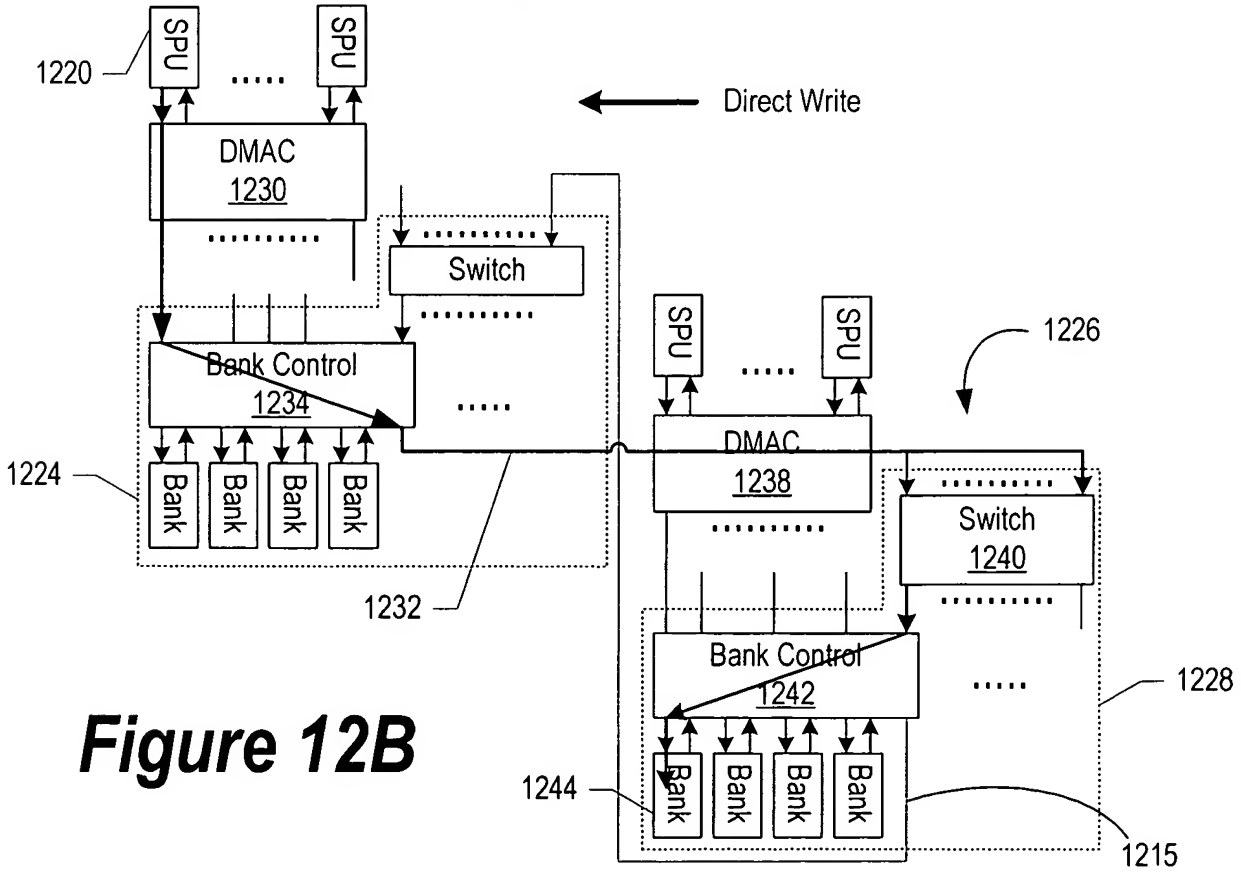

Figure 12B

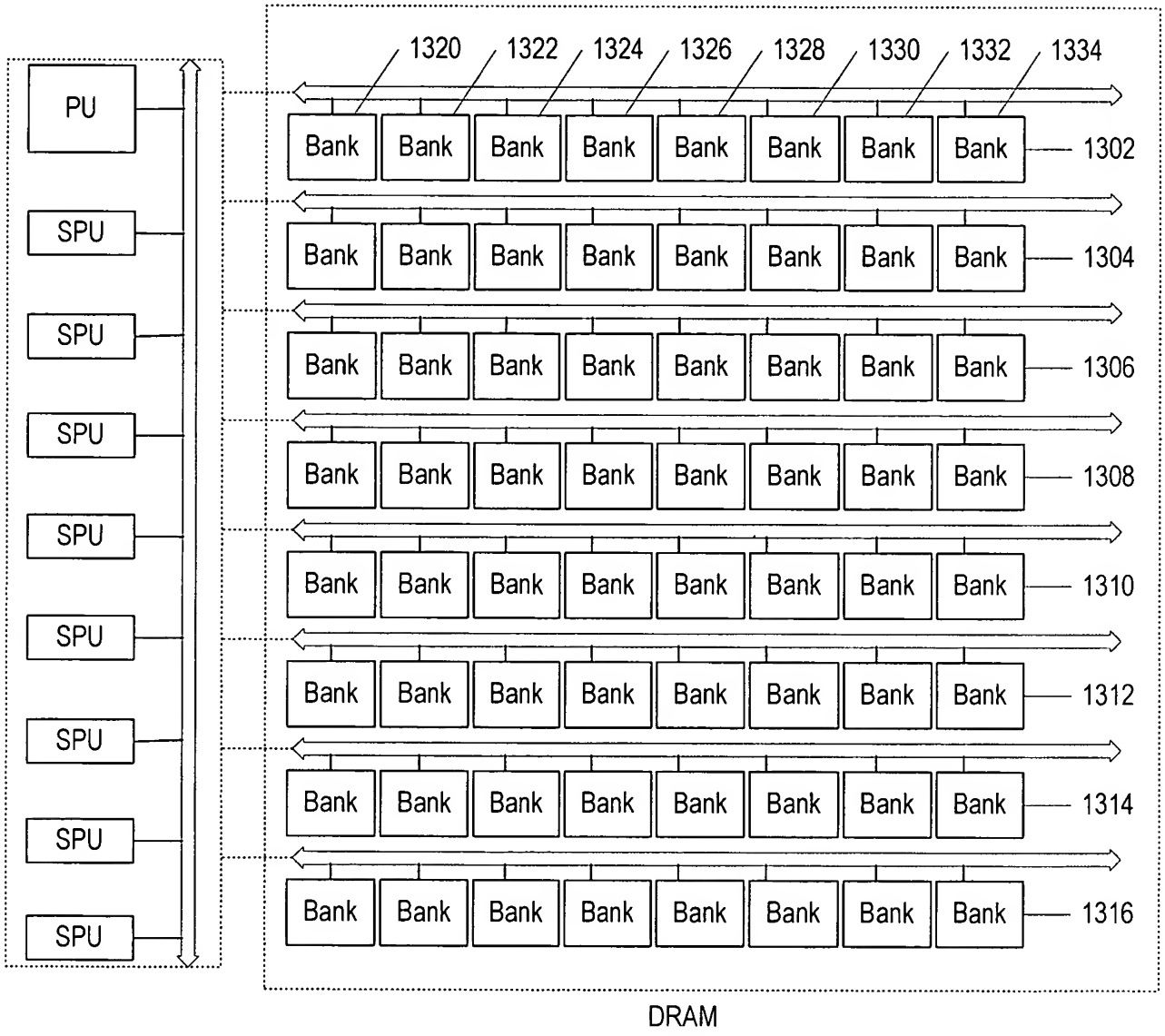
1320
1322
1324
1326
1328
1330
1332
1334
PU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
Bank
1302
1304
1306
1308
1310
1312
1314
1316
DRAM

Figure 13

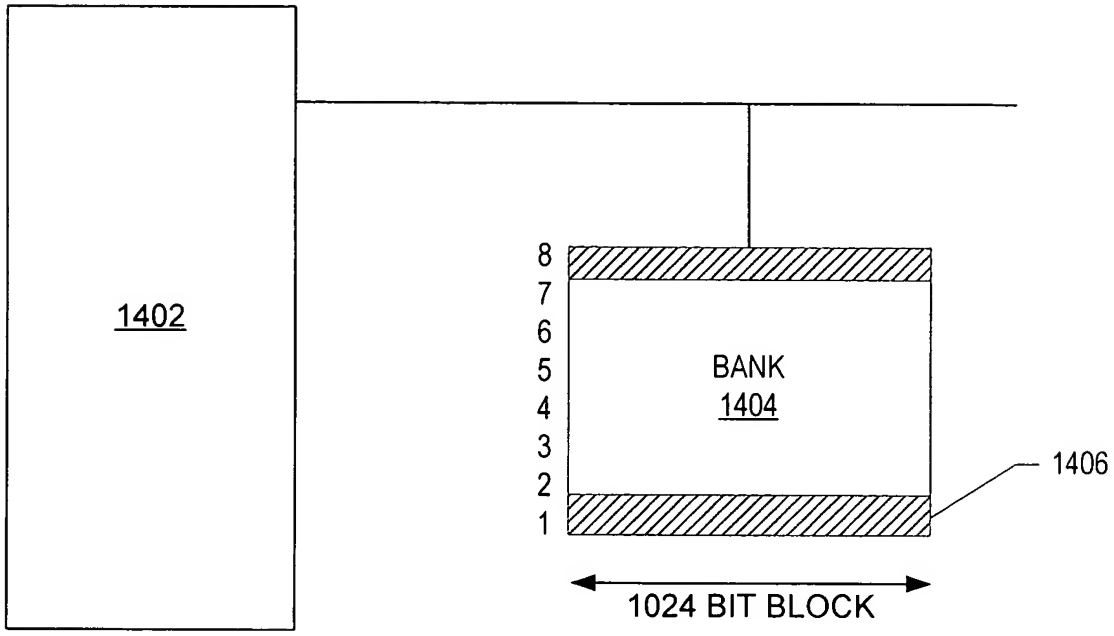

Figure 14A

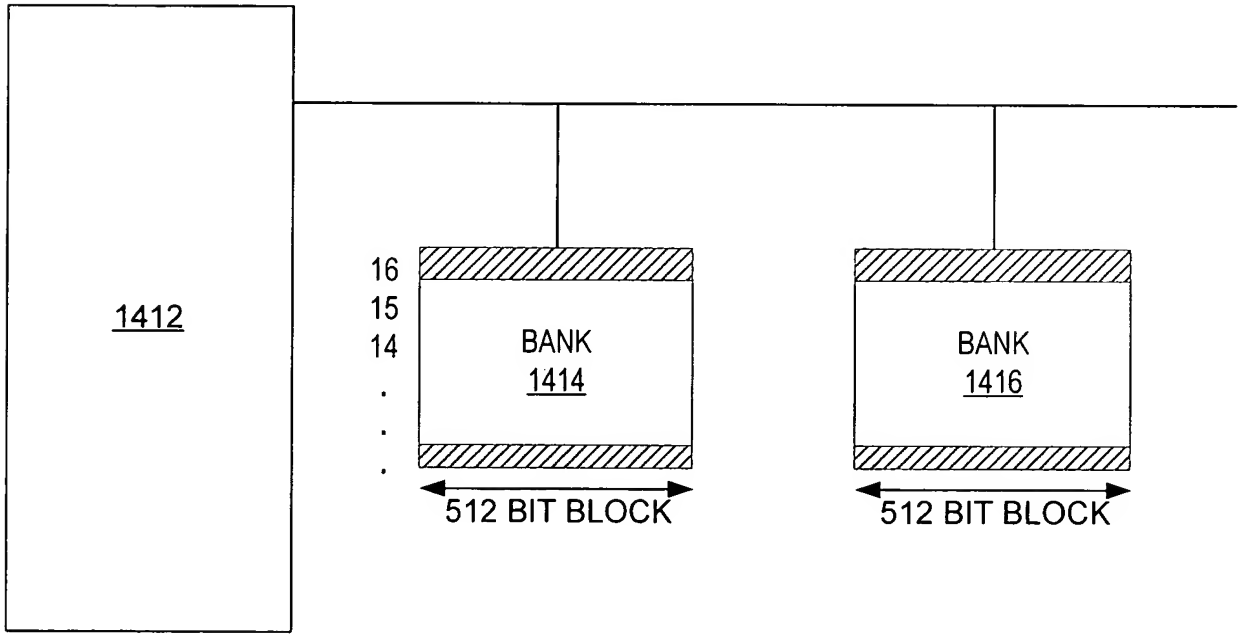

Figure 14B

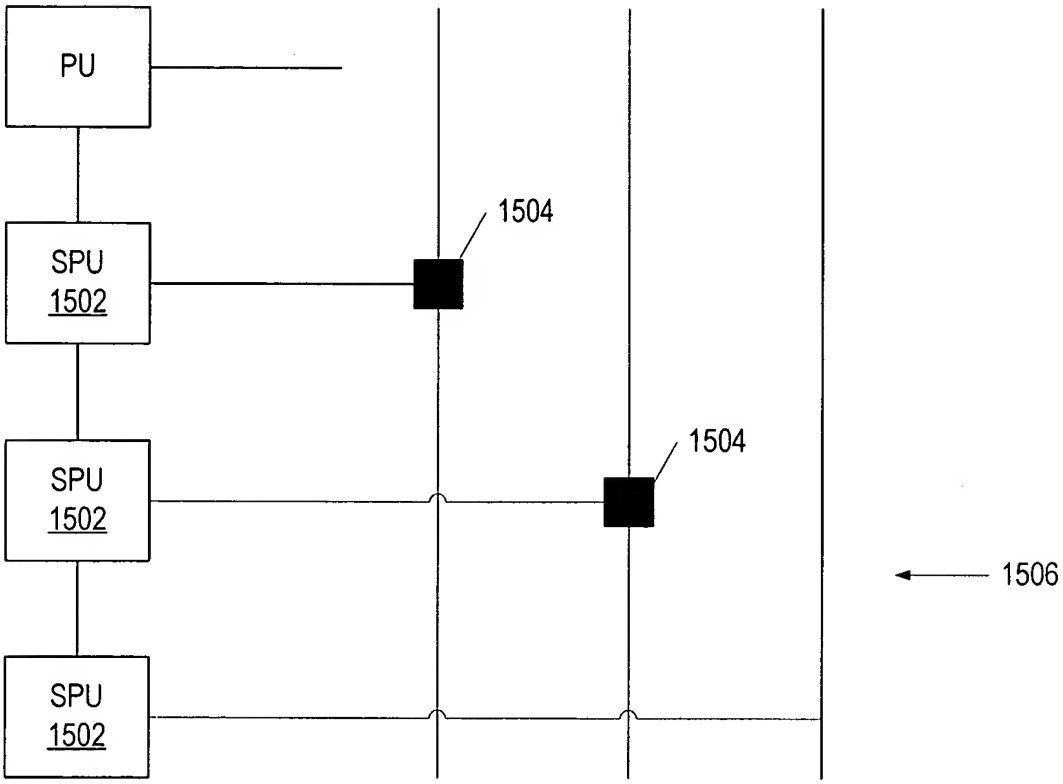

Figure 15

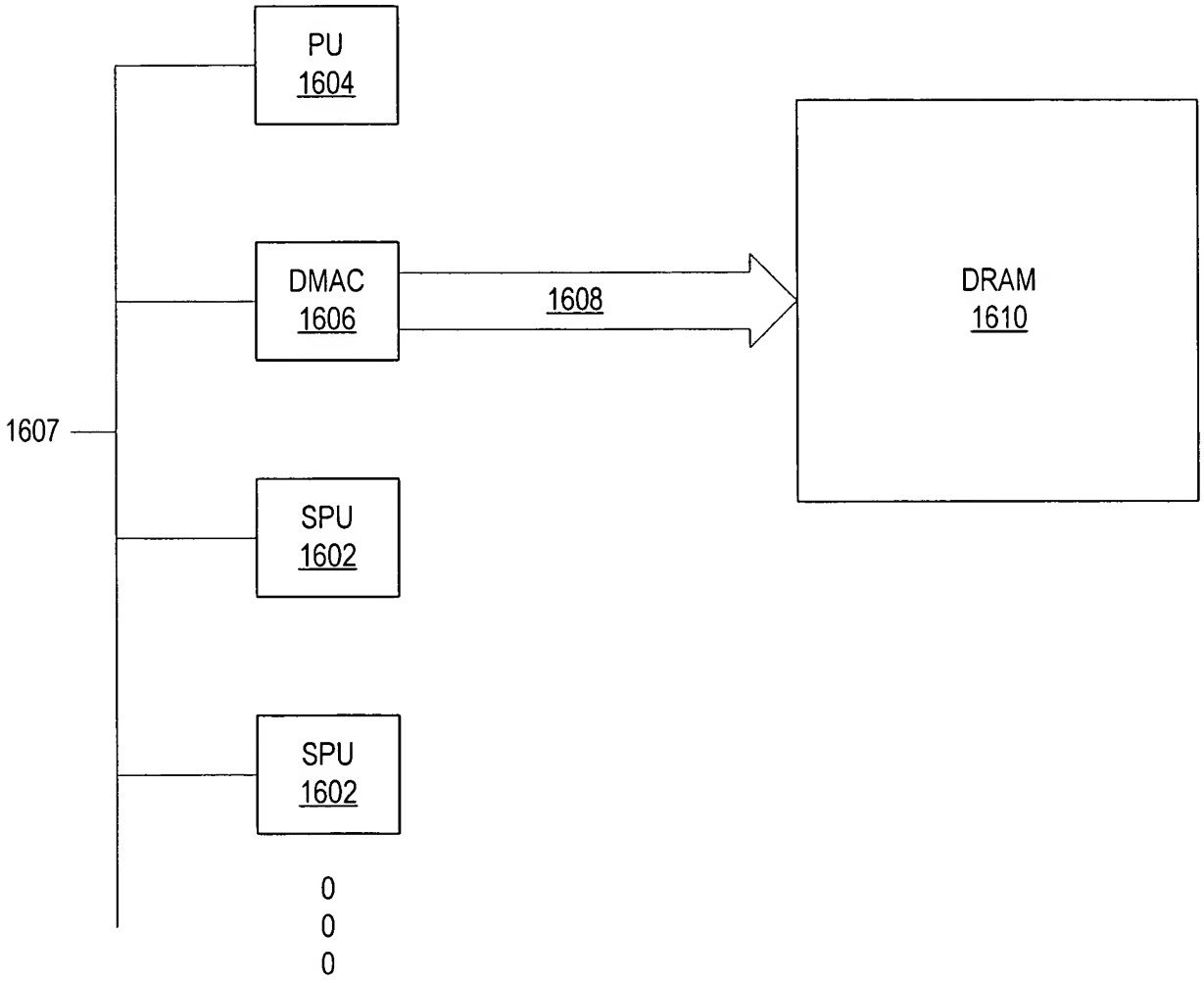

Figure 16

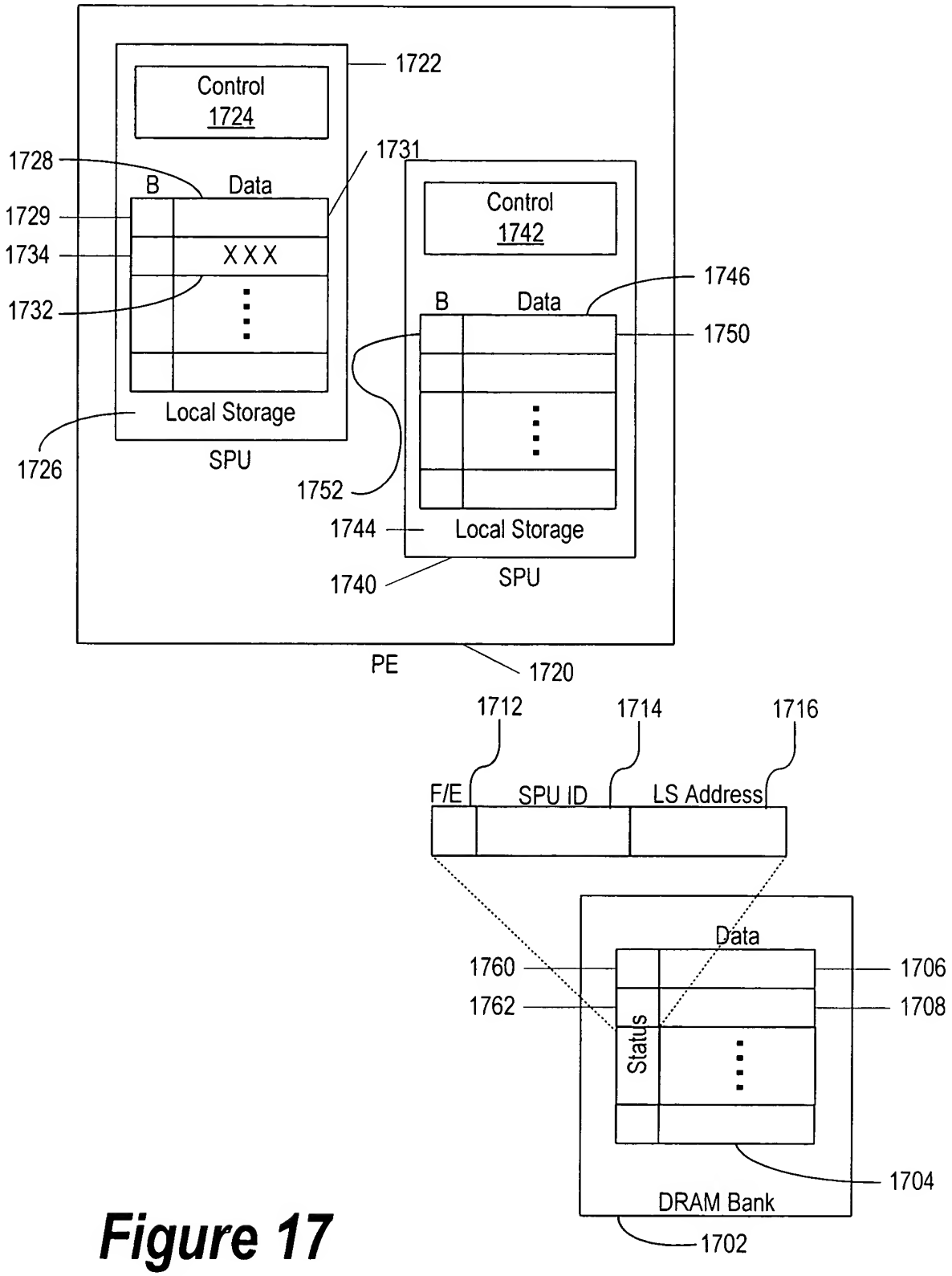
1722
Control
1724
1728
1731
B
Data
1729
1734
XXX
1732
Control
1742
1746
B
Data
1750
Local Storage
1726
SPU
1752
1744
Local Storage
1740
SPU
PE
1720
1712
1714
1716
F/E
SPU ID
LS Address
Data
1760
1762
1706
1708
Status
1704
DRAM Bank
1702

Figure 17

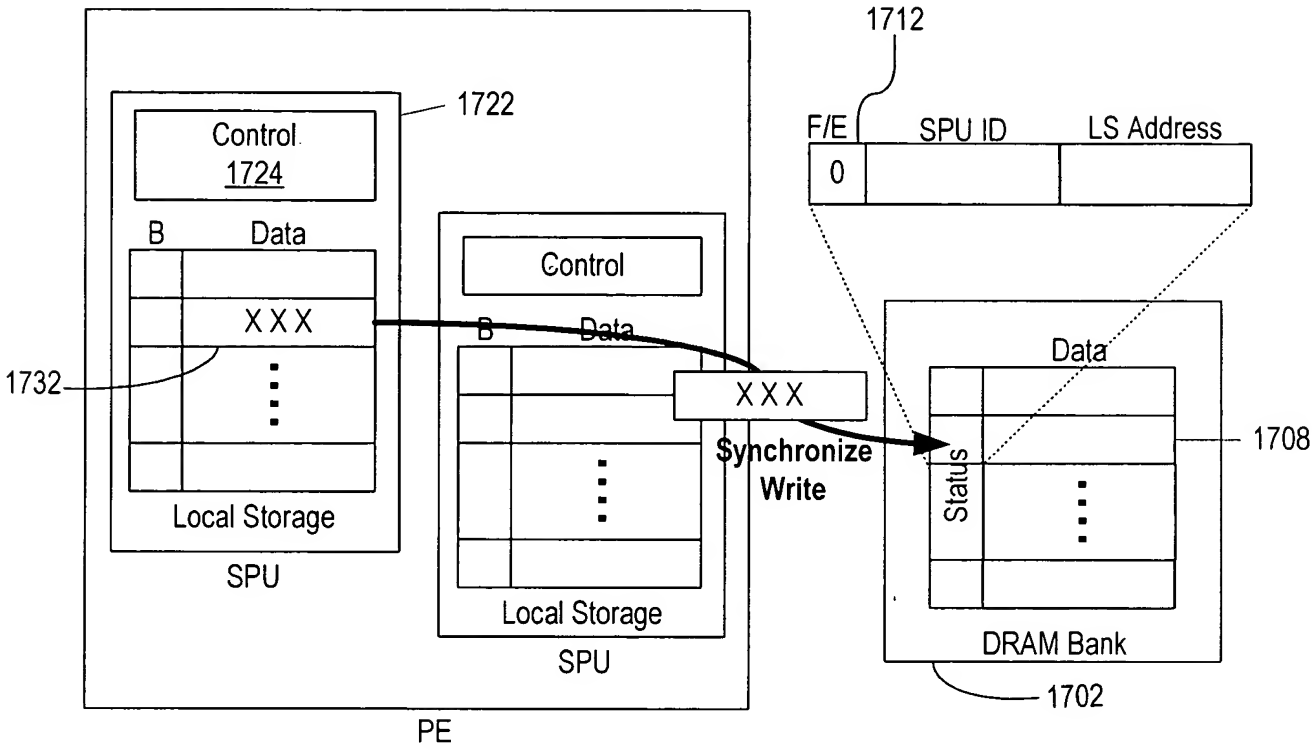
1712
F/E
SPU ID
LS Address
0
1722
Control
1724
B
Data
XXX
1732
Local Storage
SPU
Control
B
Data
XXX
Synchronize
Write
Local Storage
SPU
PE
Data
Status
1708
DRAM Bank
1702

Figure 18

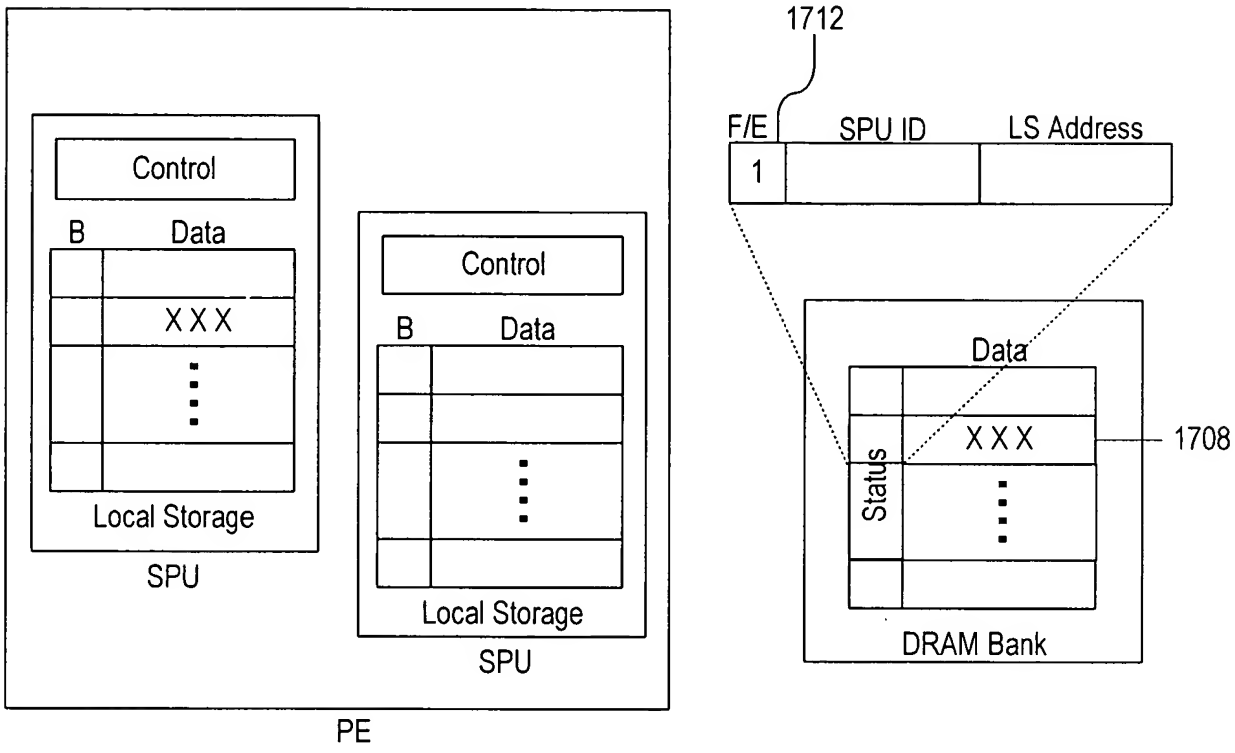
Control
B
Data
XXX
Local Storage
SPU
Control
B
Data
Local Storage
SPU
PE
1712
F/E
SPU ID
LS Address
1
Data
XXX
Status
1708
DRAM Bank

Figure 19

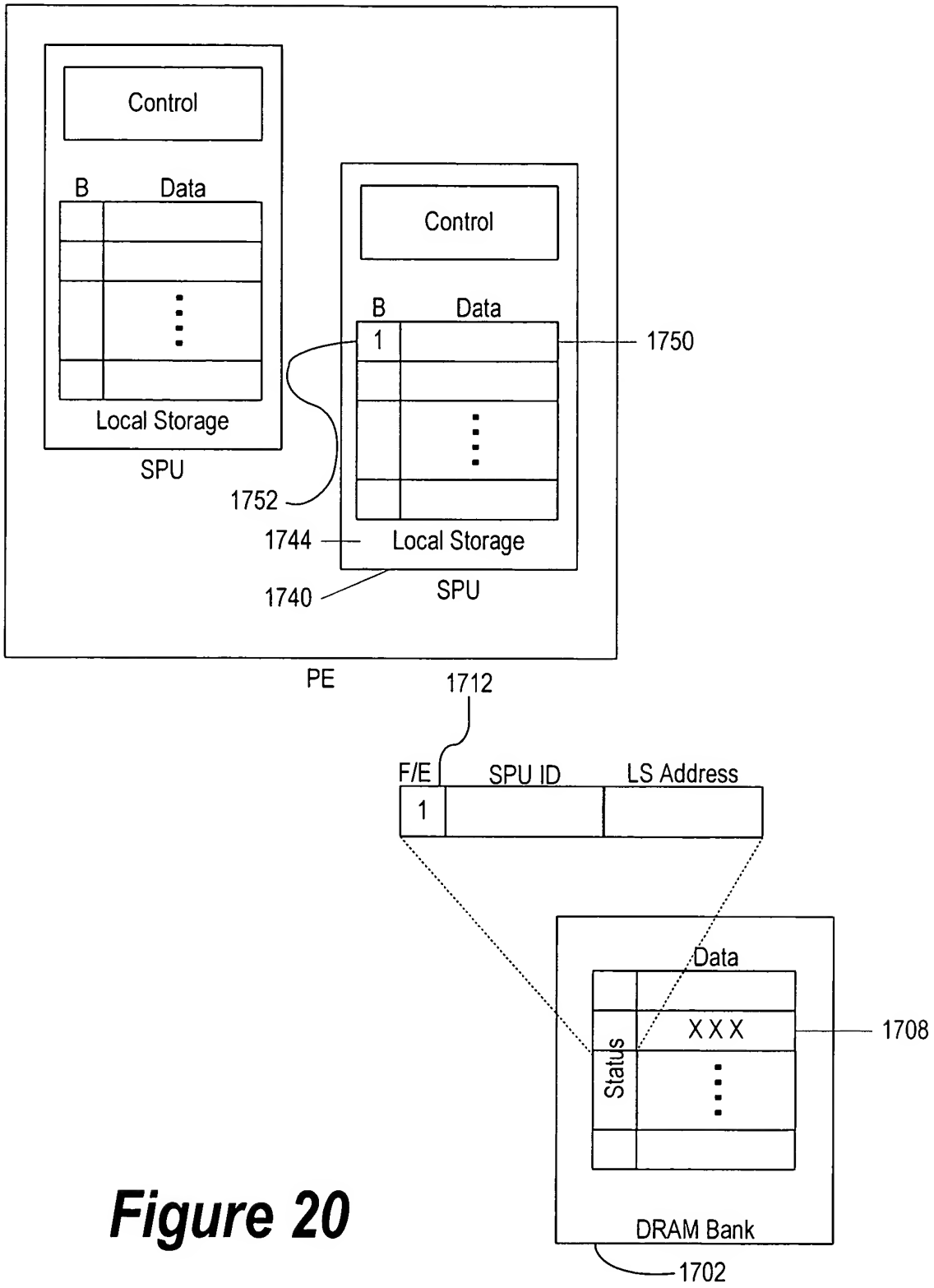
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
1
Data
XXX
1708
Status
DRAM Bank
1702

Figure 20

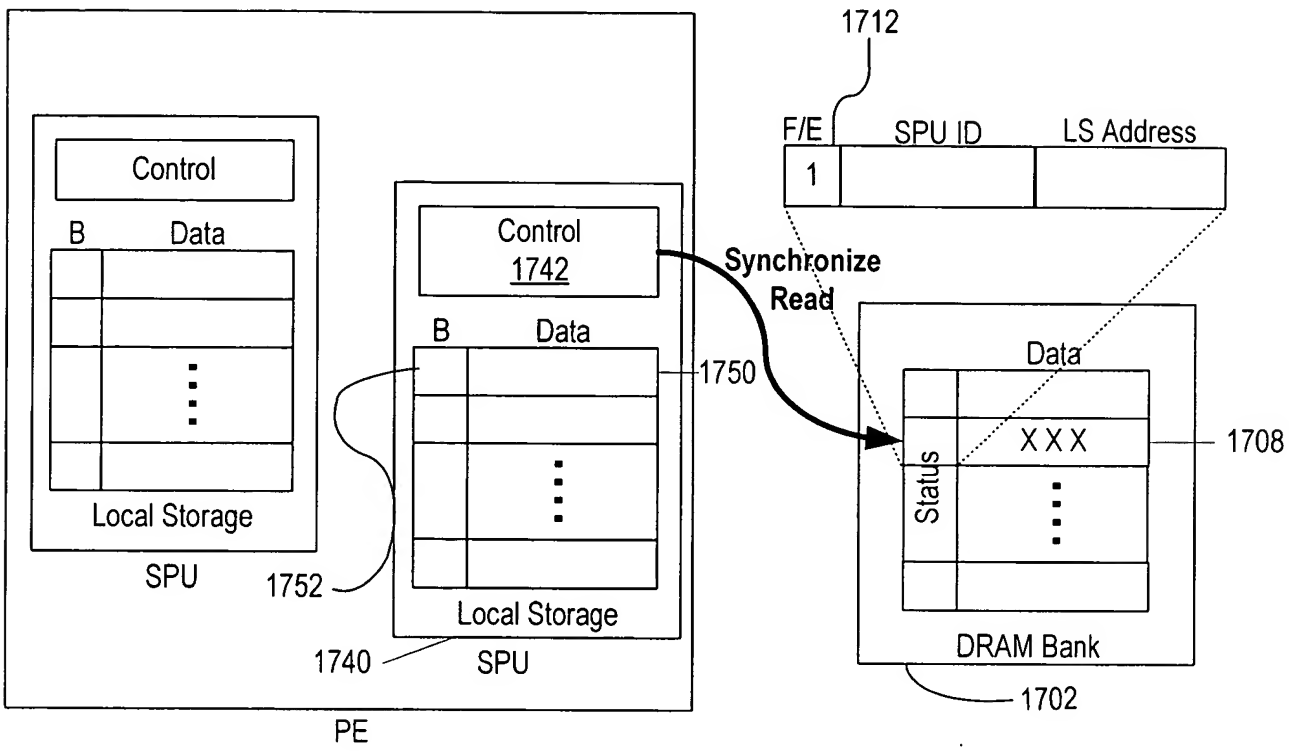
1712
F/E
SPU ID
LS Address
1
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
Data
1750
Local Storage
1740
SPU
PE
Synchronize
Read
Data
X X X
1708
Status
DRAM Bank
1702

Figure 21

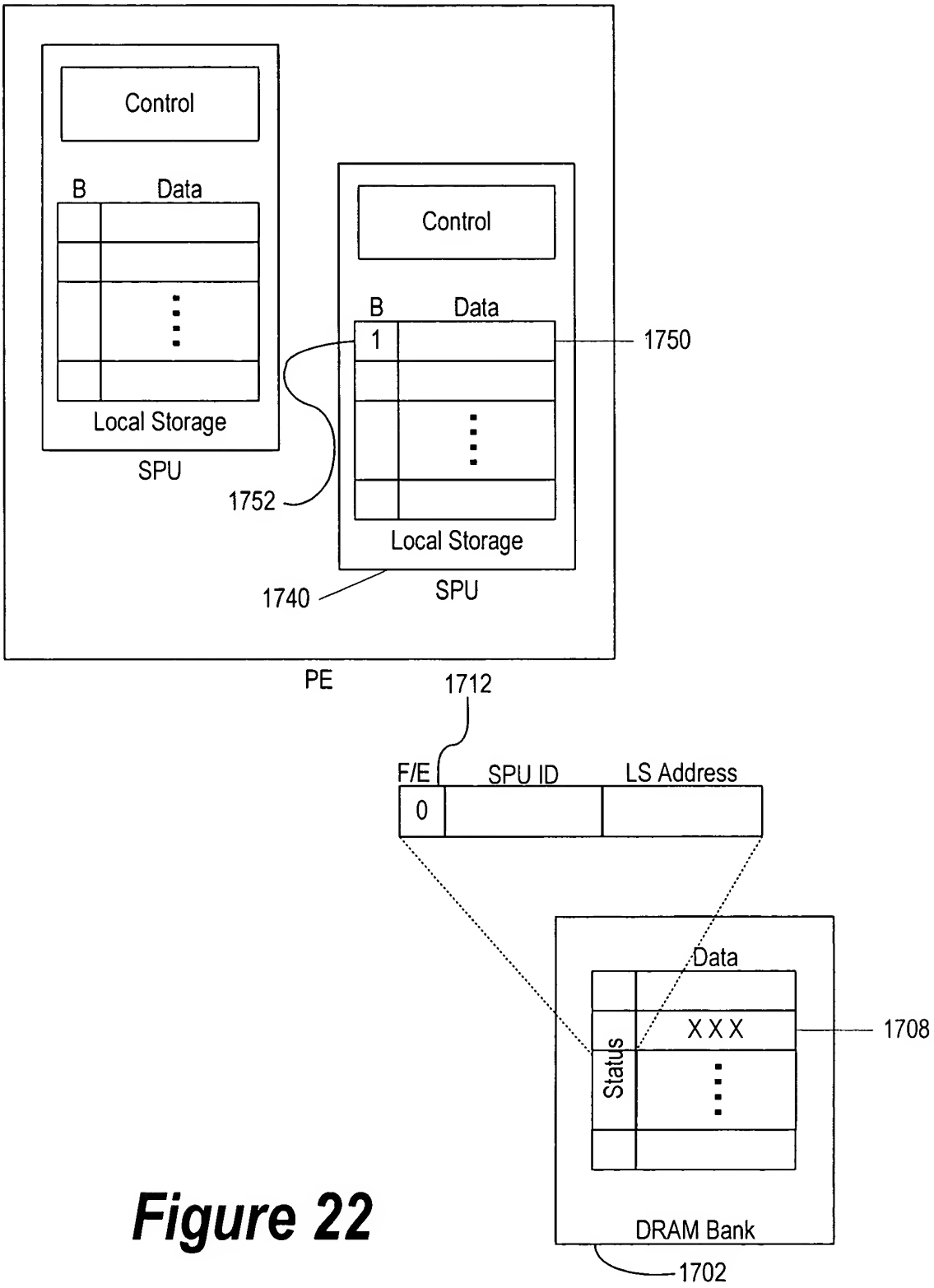
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
X X X
Status
1708
DRAM Bank
1702

Figure 22

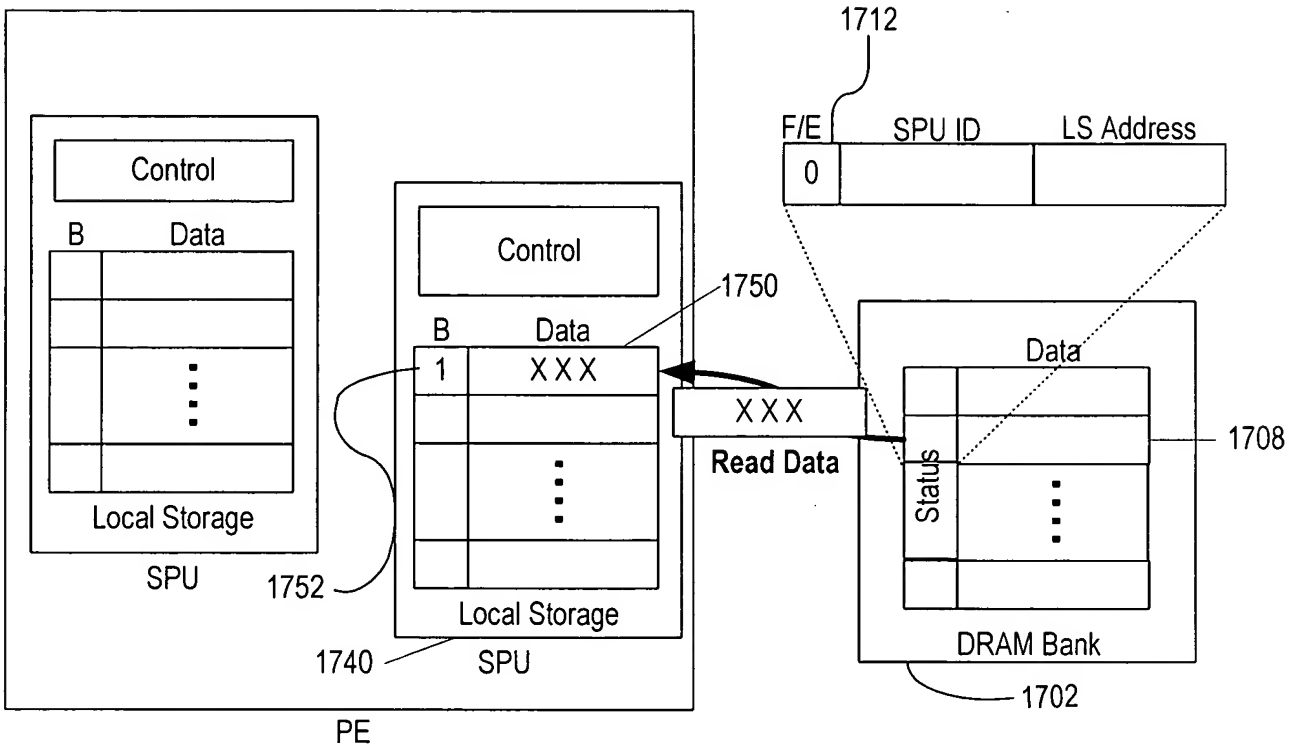
1712
F/E
SPU ID
LS Address
0
Control
B
Data
Local Storage
SPU
1752
Control
B
Data
1
XXX
1750
XXX
Read Data
Local Storage
1740
SPU
PE
Data
Status
1708
DRAM Bank
1702

Figure 23

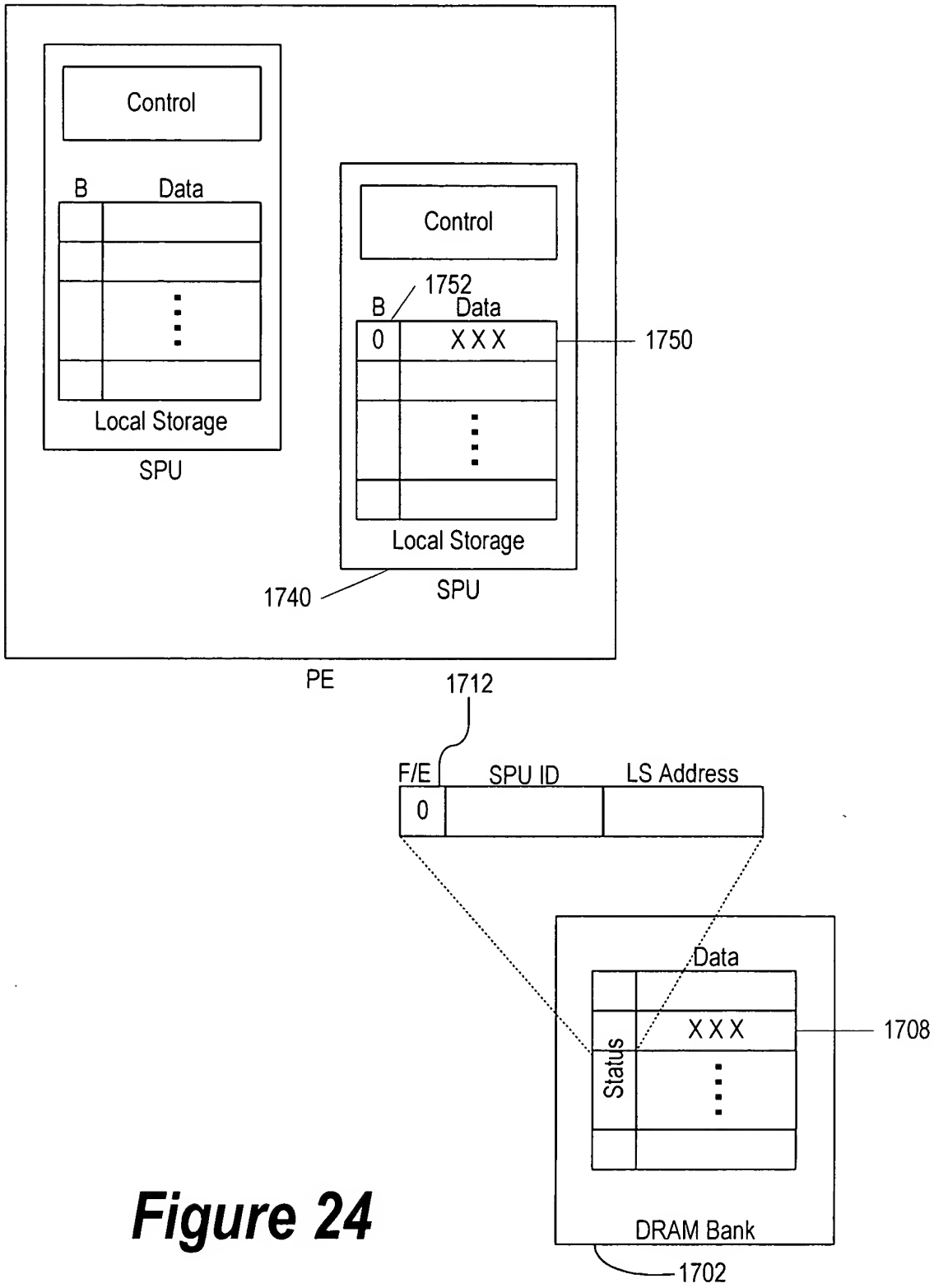
Control
B
Data
Local Storage
SPU
Control
1752
B
Data
0
X X X
1750
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
X X X
1708
Status
DRAM Bank
1702

Figure 24

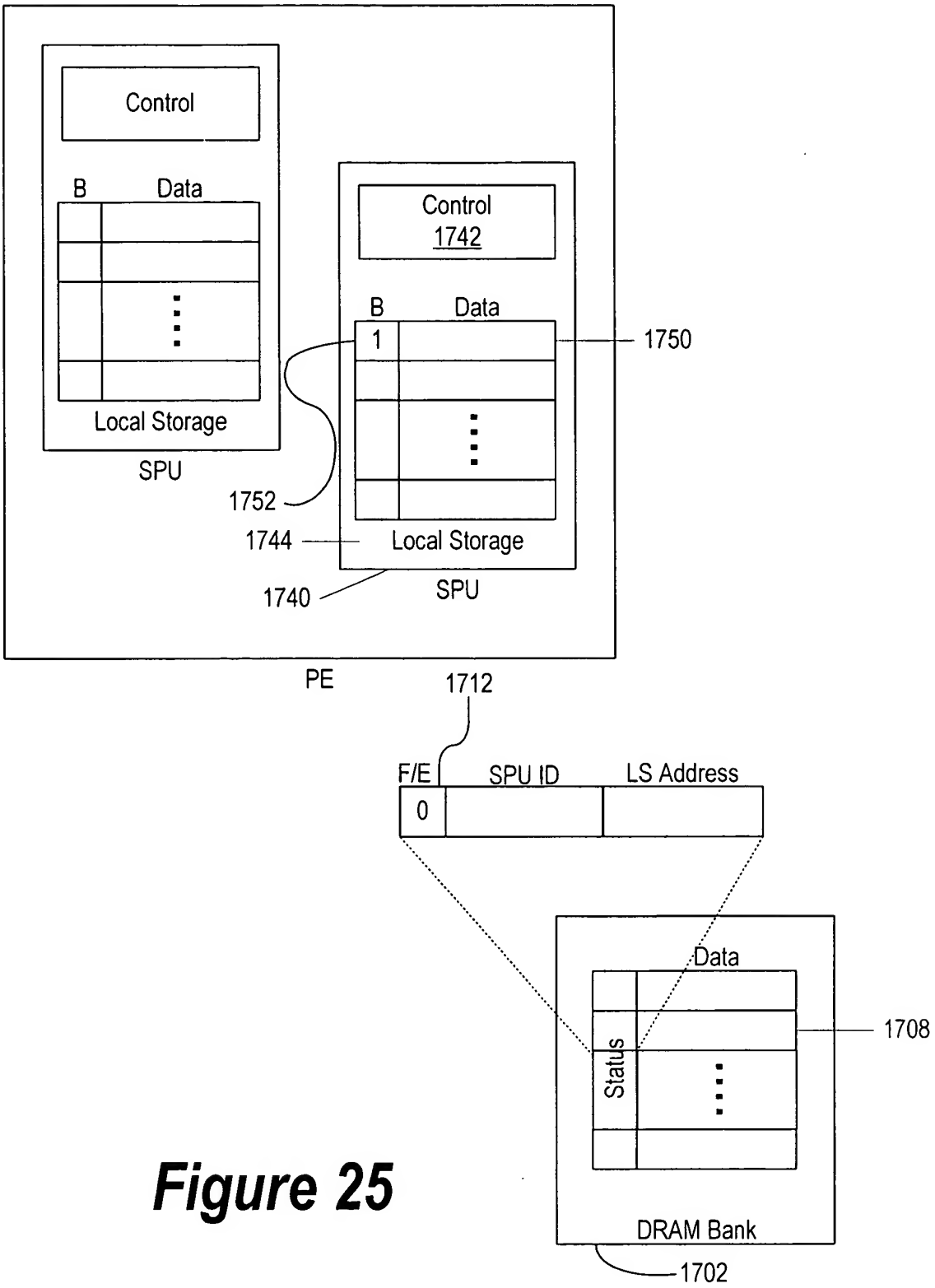
Control
B
Data
Local Storage
SPU
Control
1742
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
0
Data
Status
1708
DRAM Bank
1702

Figure 25

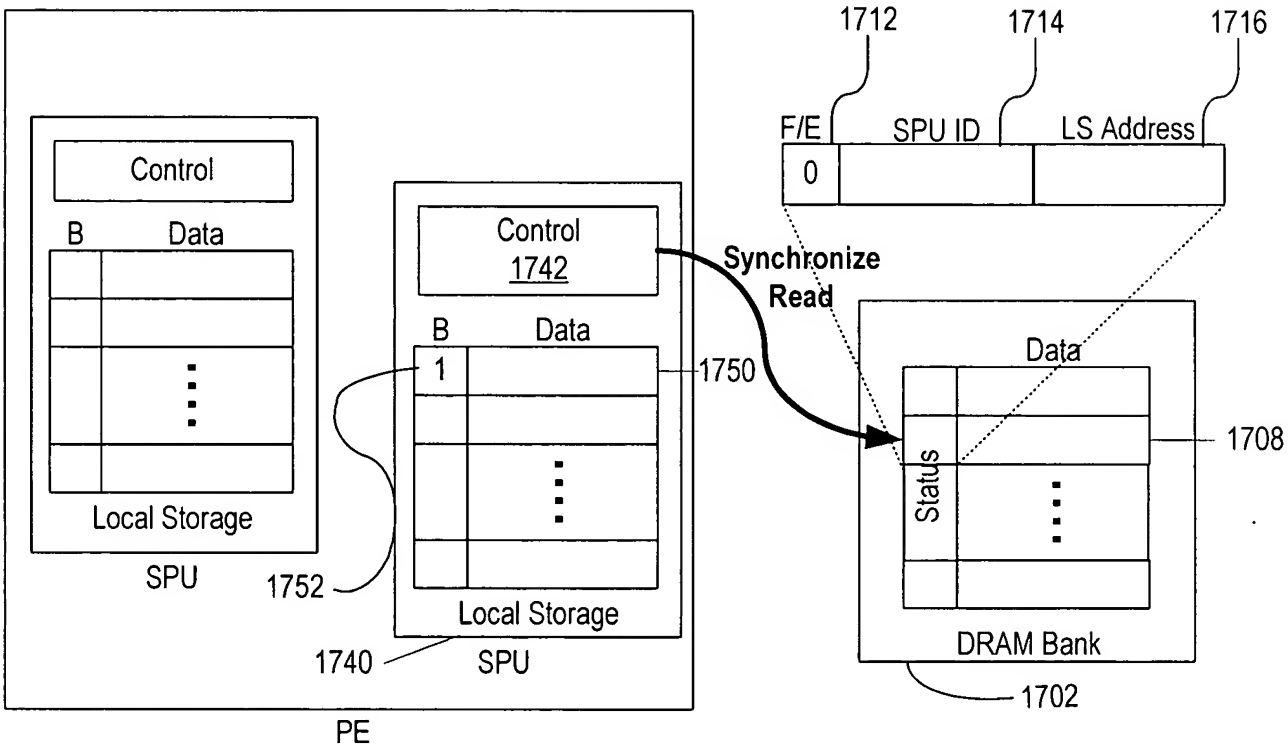
1712
1714
1716
F/E
SPU ID
LS Address
0
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
Data
1
1750
Synchronize
Read
Data
1708
Status
Local Storage
1740
SPU
DRAM Bank
1702
PE

Figure 26

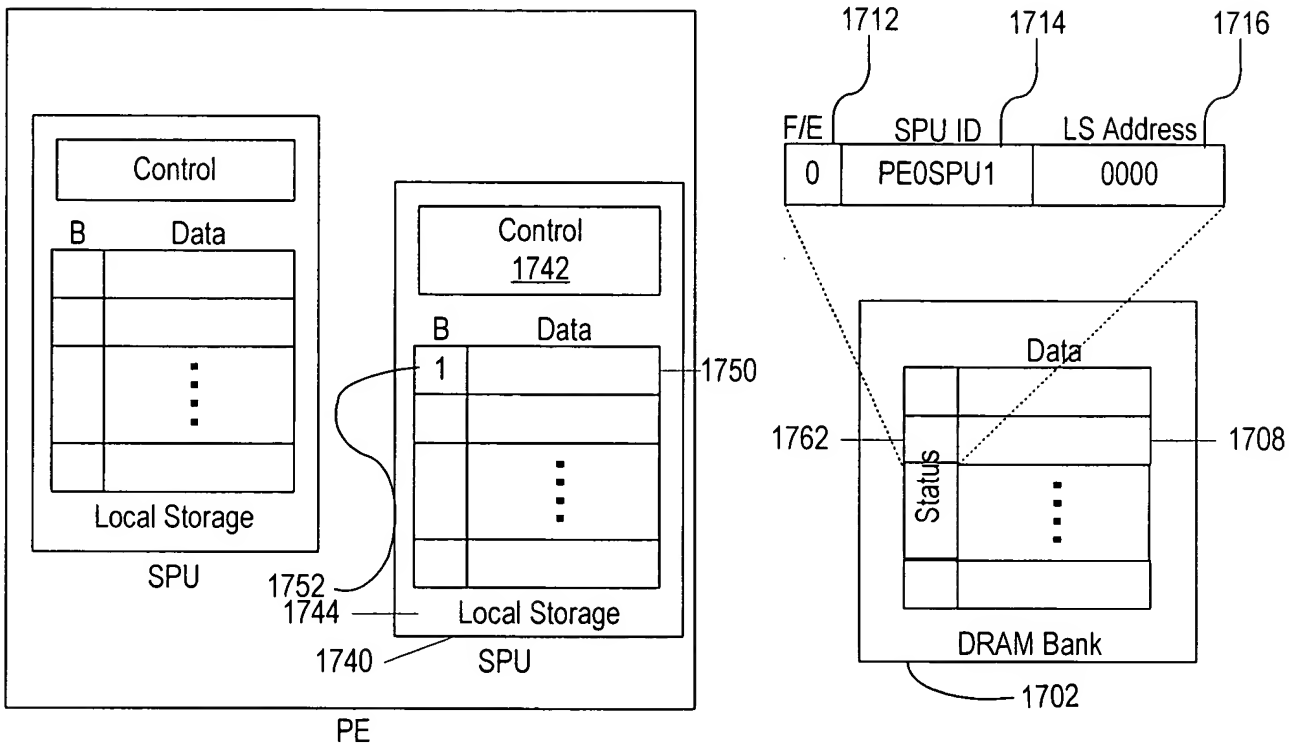
1712
1714
1716
F/E
SPU ID
LS Address
0
PE0SPU1
0000
Control
B
Data
Local Storage
SPU
Control
1742
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
Data
1762
1708
Status
DRAM Bank
1702

Figure 27

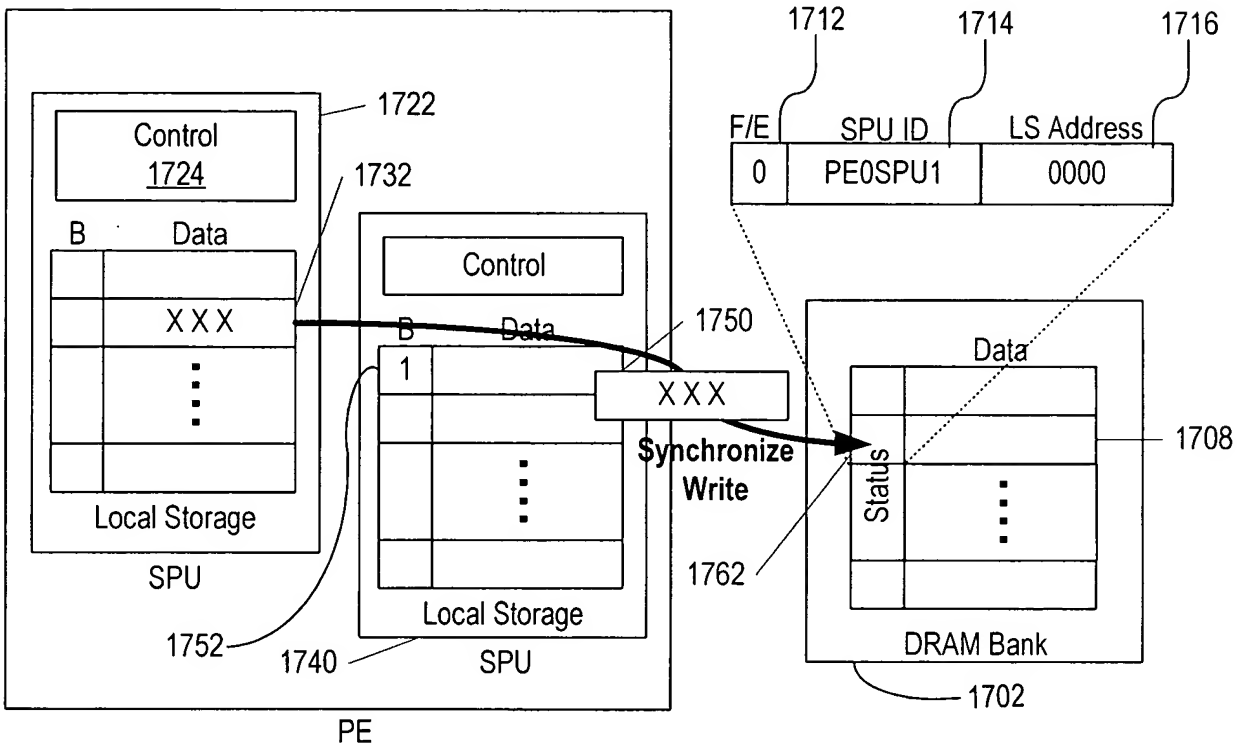
1712
1714
1716
F/E
SPU ID
LS Address
0
PE0SPU1
0000
1722
Control
1724
1732
B
Data
XXX
Local Storage
SPU
Control
B
Data
1
1750
XXX
Synchronize
Write
1762
Data
Status
1708
DRAM Bank
1702
1752
1740
Local Storage
SPU
PE

Figure 28

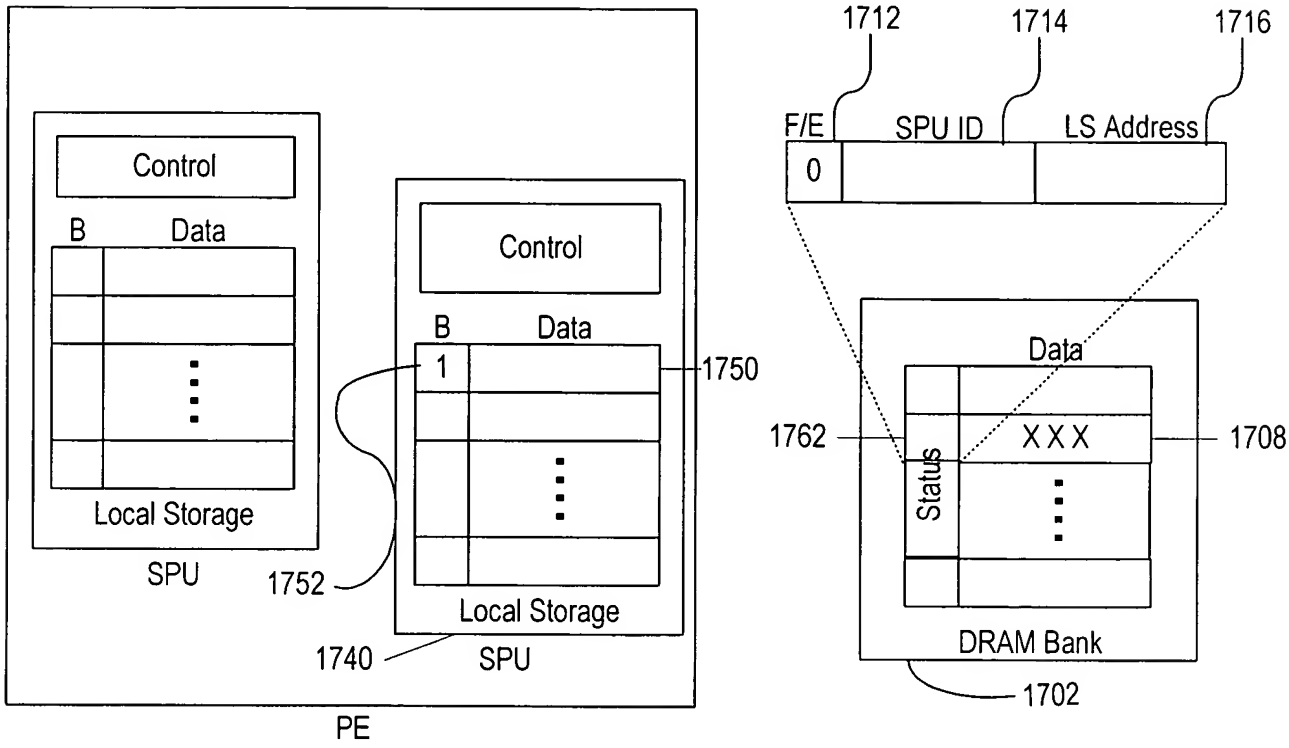
1712
1714
1716
F/E
SPU ID
LS Address
0
Control
B
Data
Local Storage
SPU
1752
Control
B
Data
1
1750
Local Storage
1740
SPU
PE
Data
1762
X X X
1708
Status
DRAM Bank
1702

Figure 29

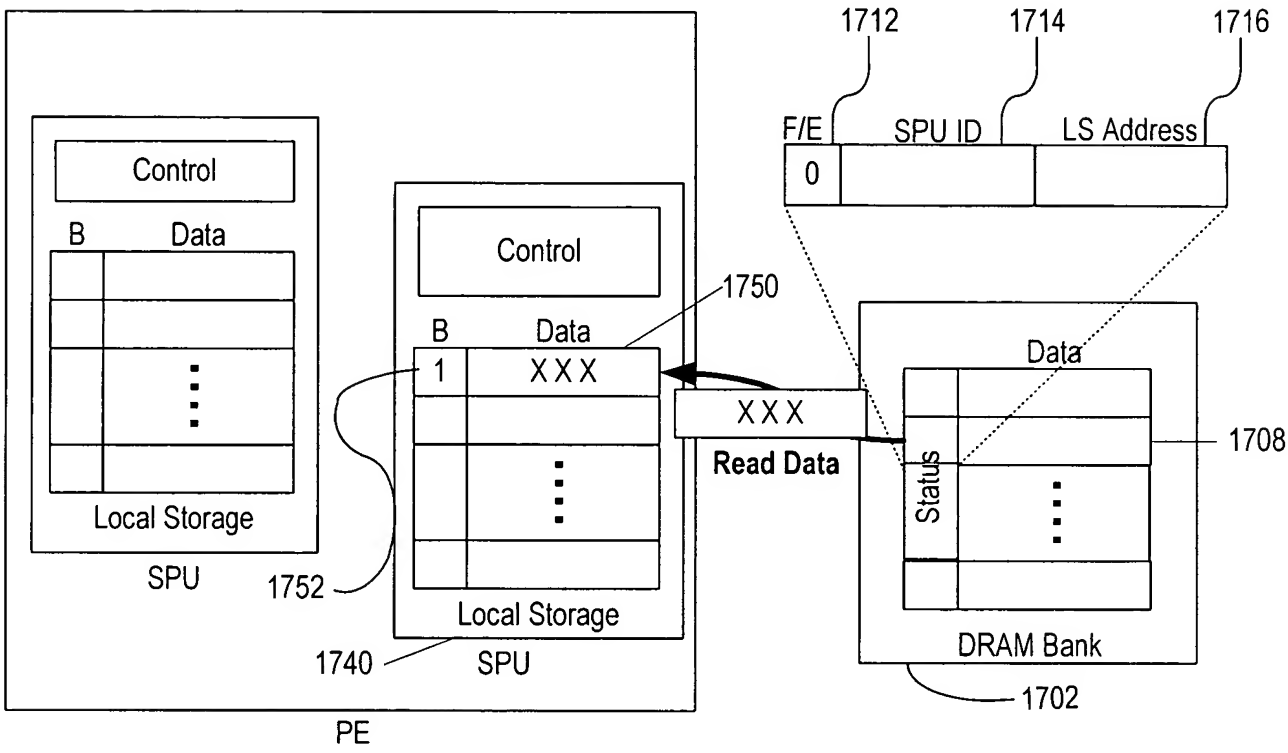
1712
1714
1716
F/E
SPU ID
LS Address
0
Control
B
Data
Local Storage
SPU
1752
Control
B
Data
1
XXX
1750
Local Storage
1740
SPU
PE
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 30

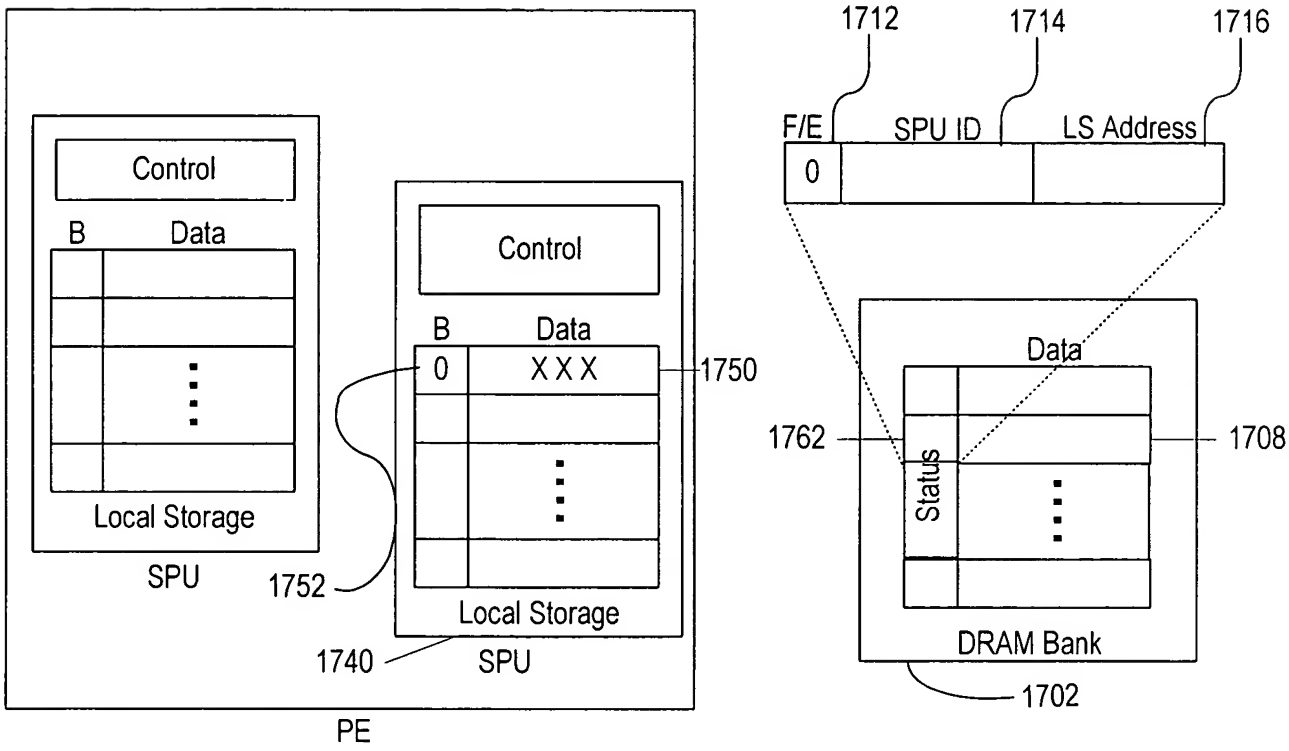
1712
1714
1716
F/E
SPU ID
LS Address
0
Control
B
Data
Local Storage
SPU
1752
Control
B
Data
0
X X X
1750
Local Storage
1740
SPU
PE
Data
1762
1708
Status
DRAM Bank
1702

Figure 31

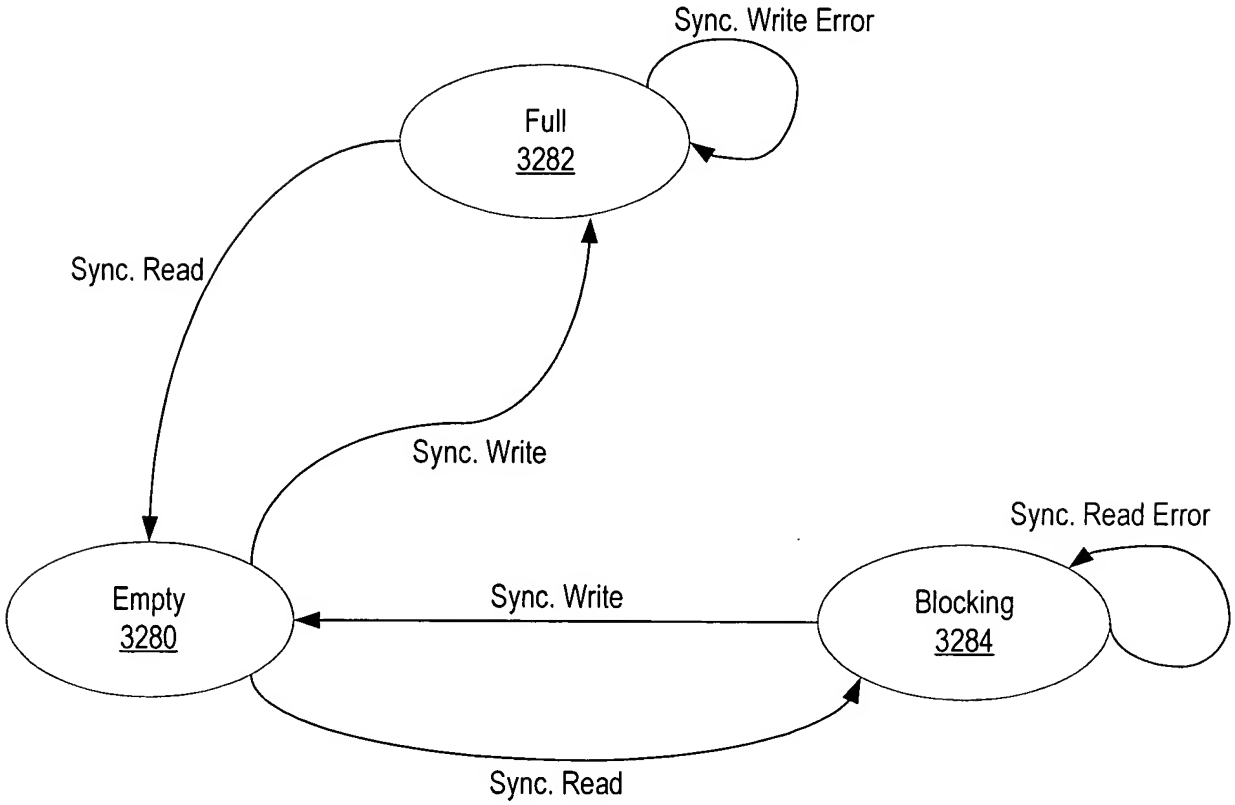
Sync. Write Error
Full
3282
Sync. Read
Sync. Write
Sync. Read Error
Empty
3280
Sync. Write
Blocking
3284
Sync. Read

Figure 32

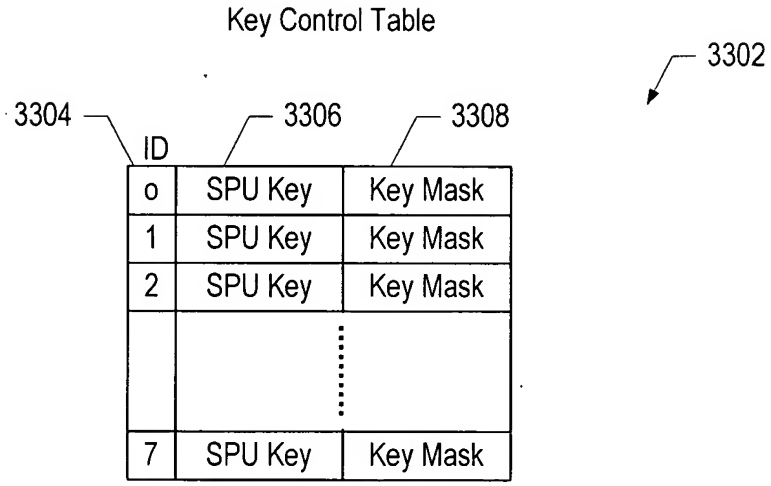
Key Control Table
3302
3304
3306
3308
ID
0
SPU Key
Key Mask
1
SPU Key
Key Mask
2
SPU Key
Key Mask
7
SPU Key
Key Mask

Figure 33

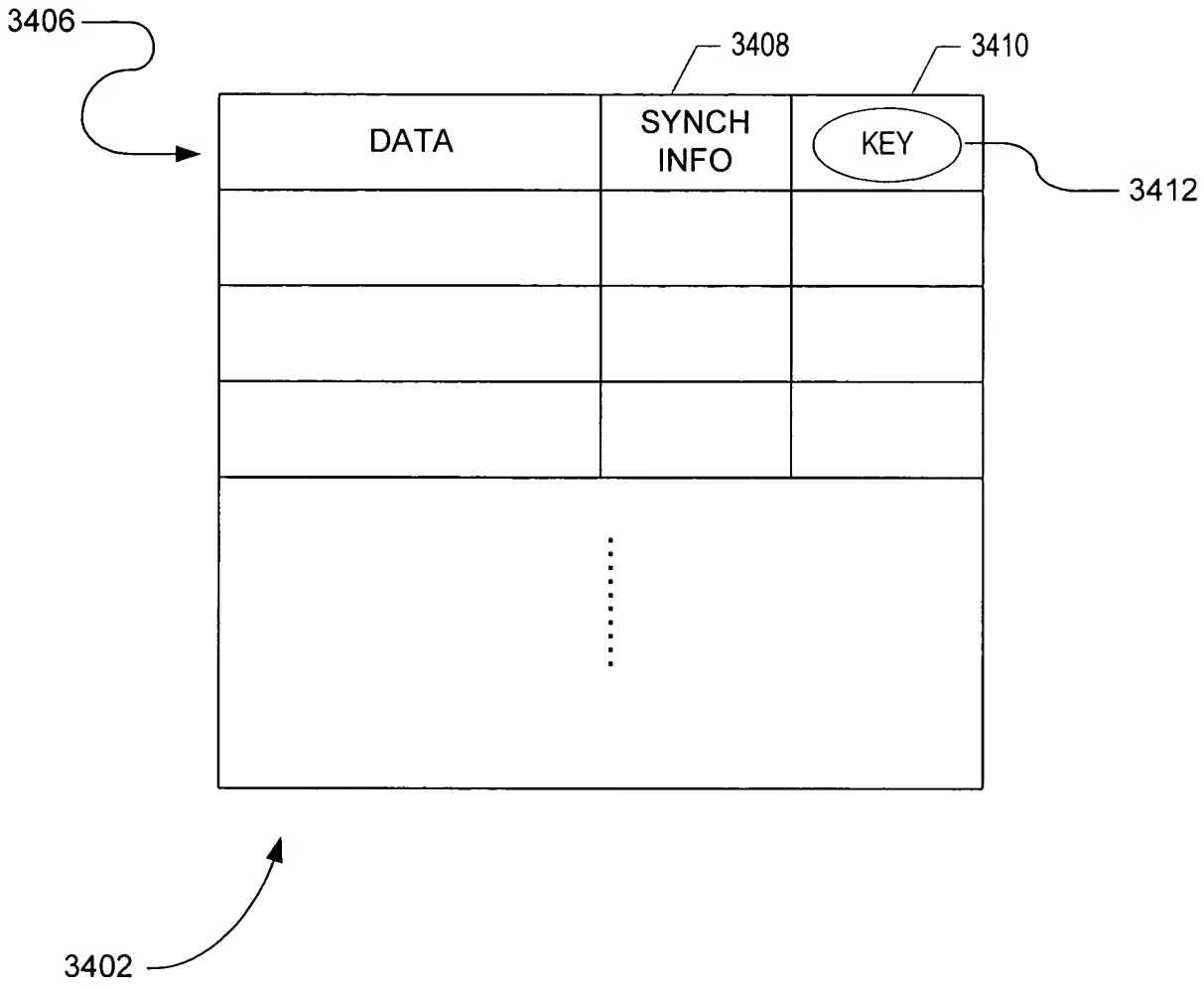

Figure 34

Memory Access Control Table

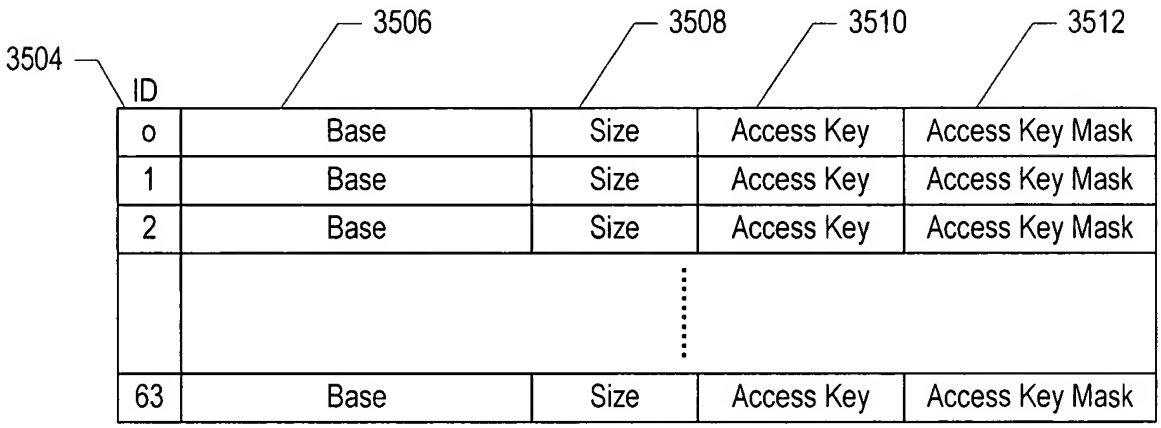

Figure 35

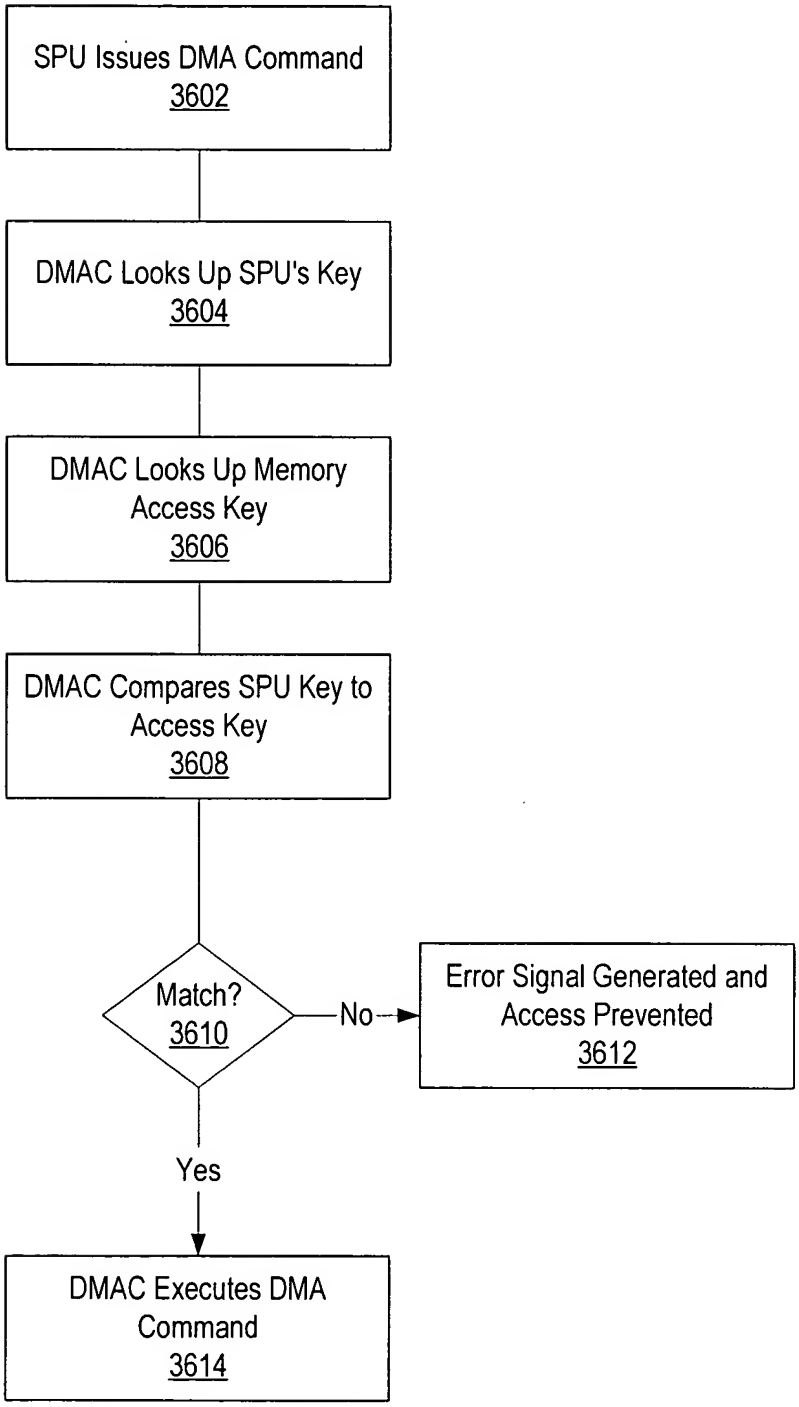
SPU Issues DMA Command
3602
DMAC Looks Up SPU's Key
3604
DMAC Looks Up Memory Access Key
3606
DMAC Compares SPU Key to Access Key
3608
Match?
3610
No
Error Signal Generated and Access Prevented
3612
Yes
DMAC Executes DMA Command
3614

Figure 36

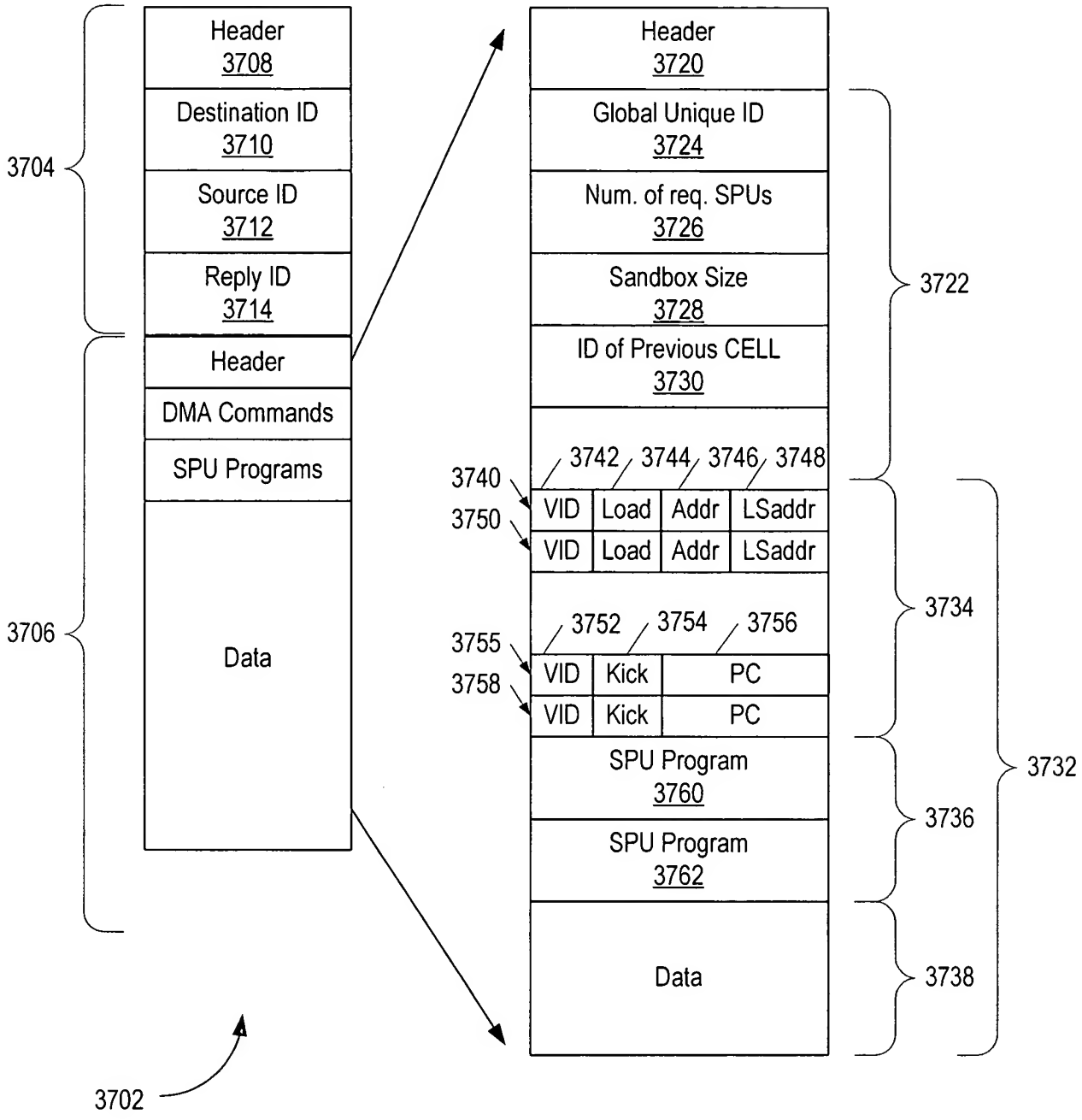
Header
3708
Destination ID
3710
Source ID
3712
Reply ID
3714
Header
DMA Commands
SPU Programs
Data
3704
3706
3702
Header
3720
Global Unique ID
3724
Num. of req. SPUs
3726
Sandbox Size
3728
ID of Previous CELL
3730
3722
3742
3744
3746
3748
3740
3750
VID
Load
Addr
LSaddr
VID
Load
Addr
LSaddr
3734
3752
3754
3756
3755
3758
VID
Kick
PC
VID
Kick
PC
SPU Program
3760
SPU Program
3762
3736
Data
3738
3732

Figure 37

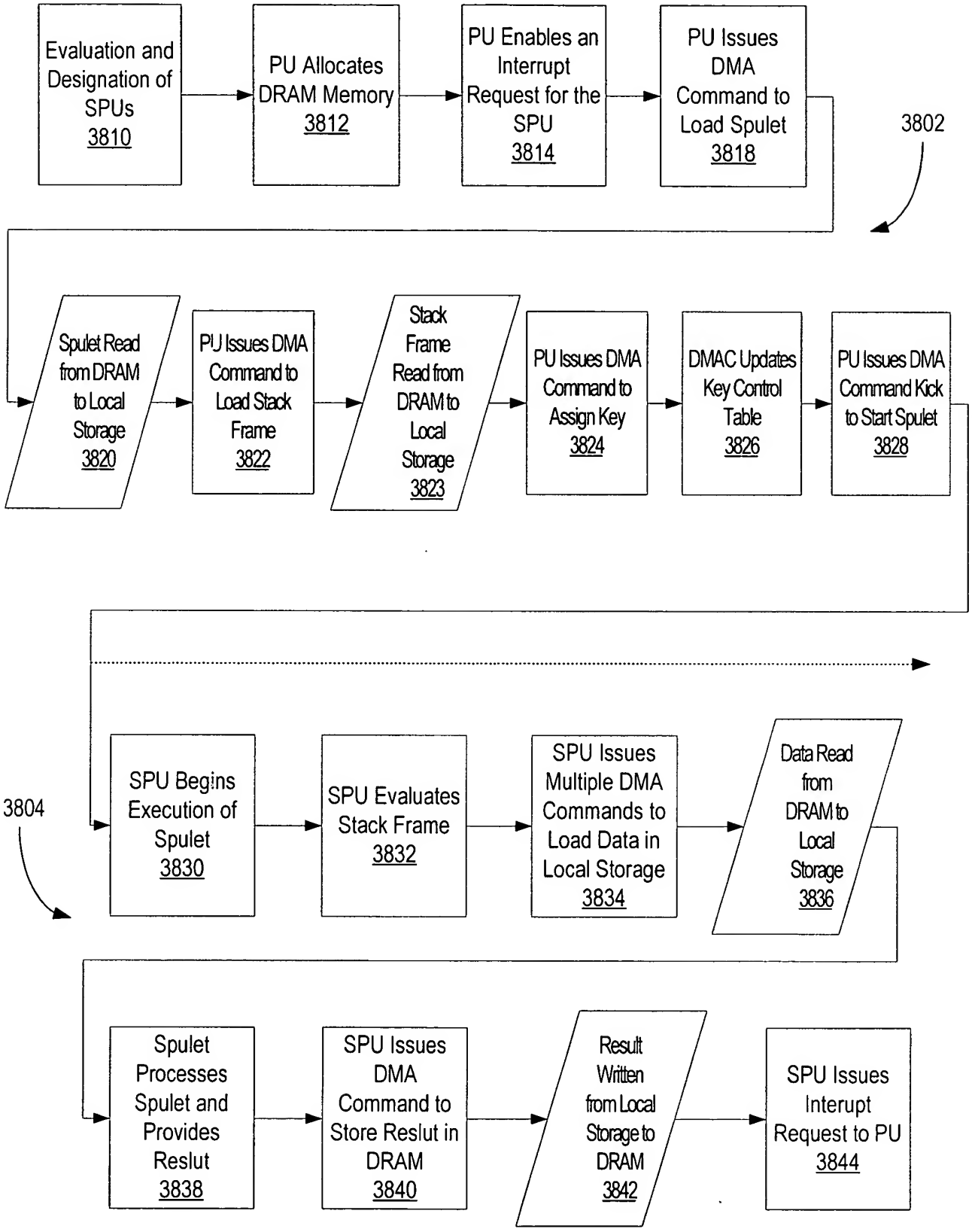
Evaluation and Designation of SPUs 3810
PU Allocates DRAM Memory 3812
PU Enables an Interrupt Request for the SPU 3814
PU Issues DMA Command to Load Spulet 3818
3802
Spulet Read from DRAM to Local Storage 3820
PU Issues DMA Command to Load Stack Frame 3822
Stack Frame Read from DRAM to Local Storage 3823
PU Issues DMA Command to Assign Key 3824
DMAC Updates Key Control Table 3826
PU Issues DMA Command Kick to Start Spulet 3828
3804
SPU Begins Execution of Spulet 3830
SPU Evaluates Stack Frame 3832
SPU Issues Multiple DMA Commands to Load Data in Local Storage 3834
Data Read from DRAM to Local Storage 3836
Spulet Processes Spulet and Provides Reslut 3838
SPU Issues DMA Command to Store Reslut in DRAM 3840
Result Written from Local Storage to DRAM 3842
SPU Issues Interupt Request to PU 3844

Figure 38

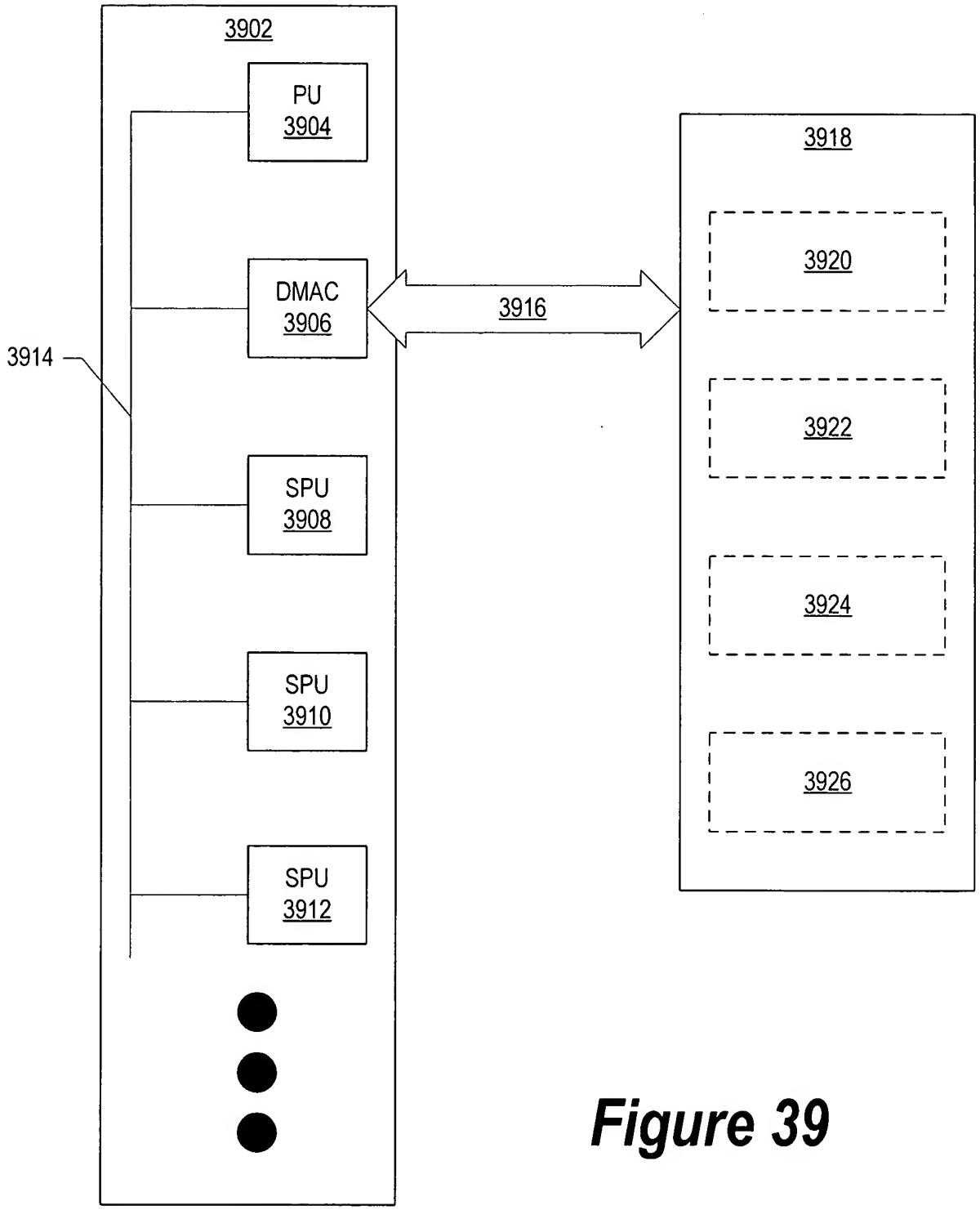
3902
PU
3904
DMAC
3906
3914
SPU
3908
SPU
3910
SPU
3912
3916
3918
3920
3922
3924
3926

Figure 39

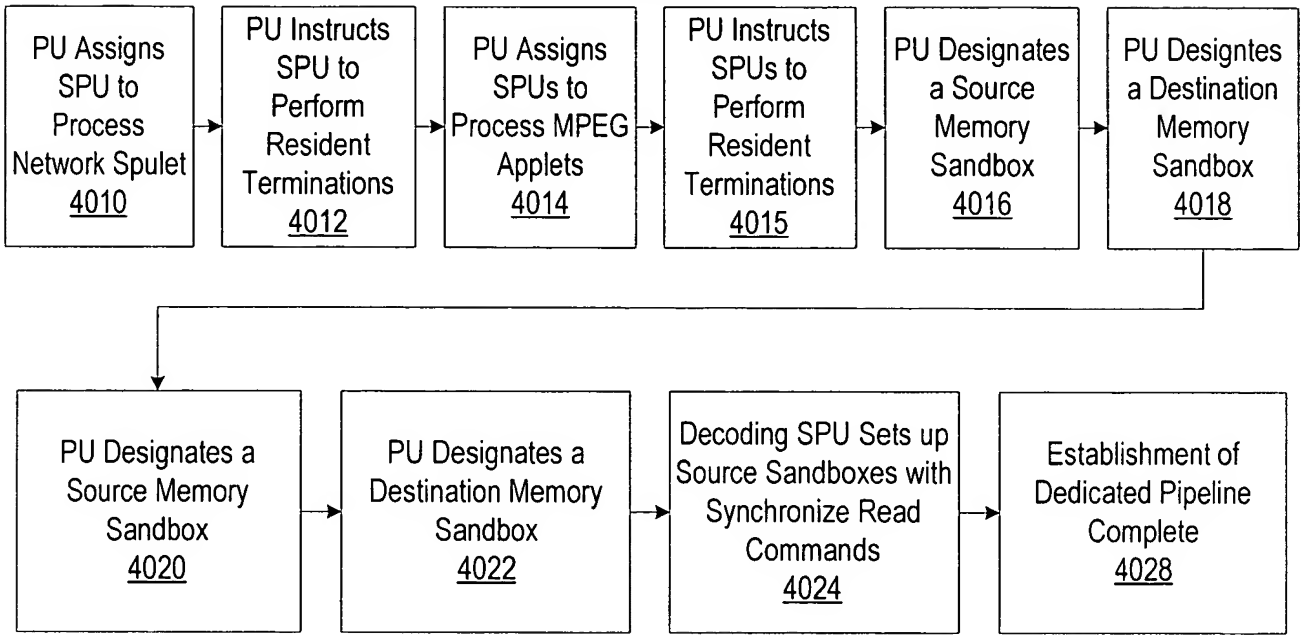

Figure 40A

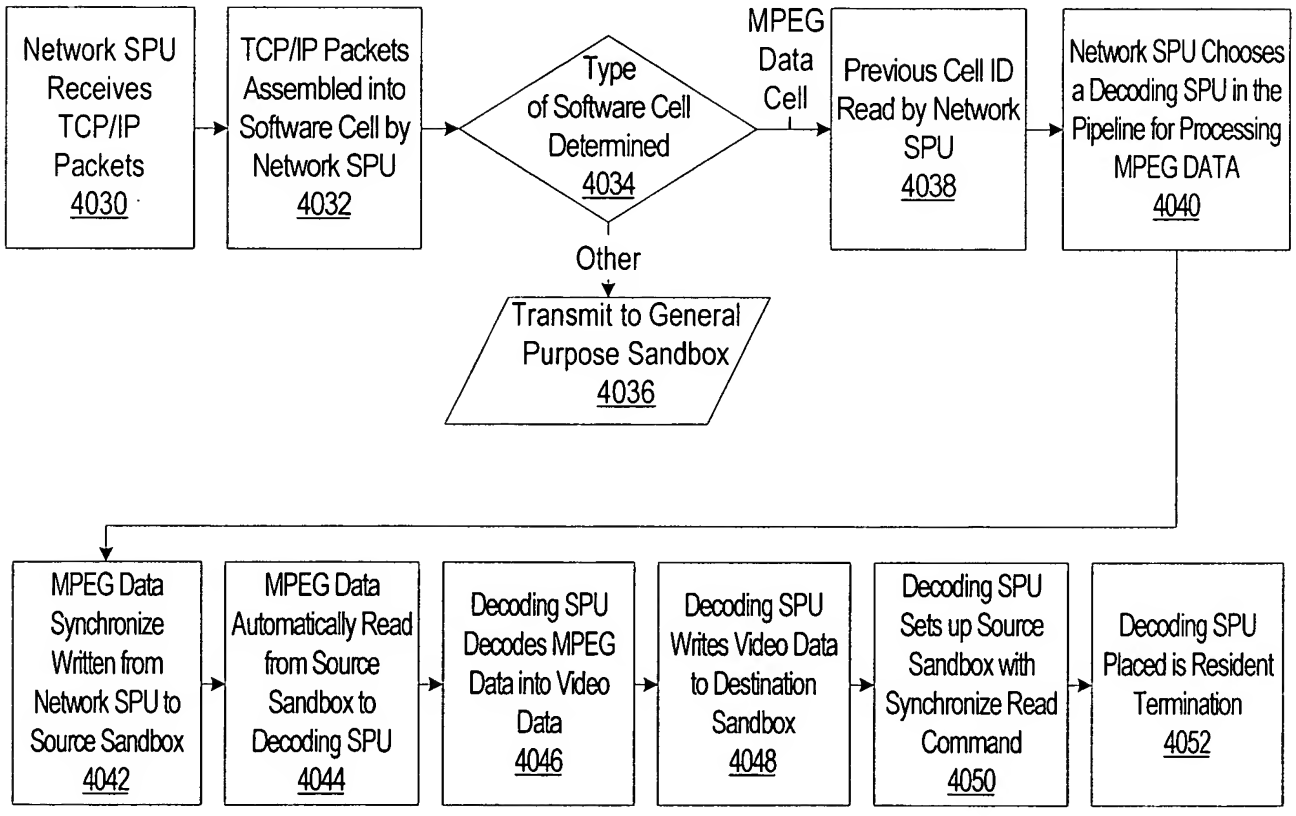

Figure 40B

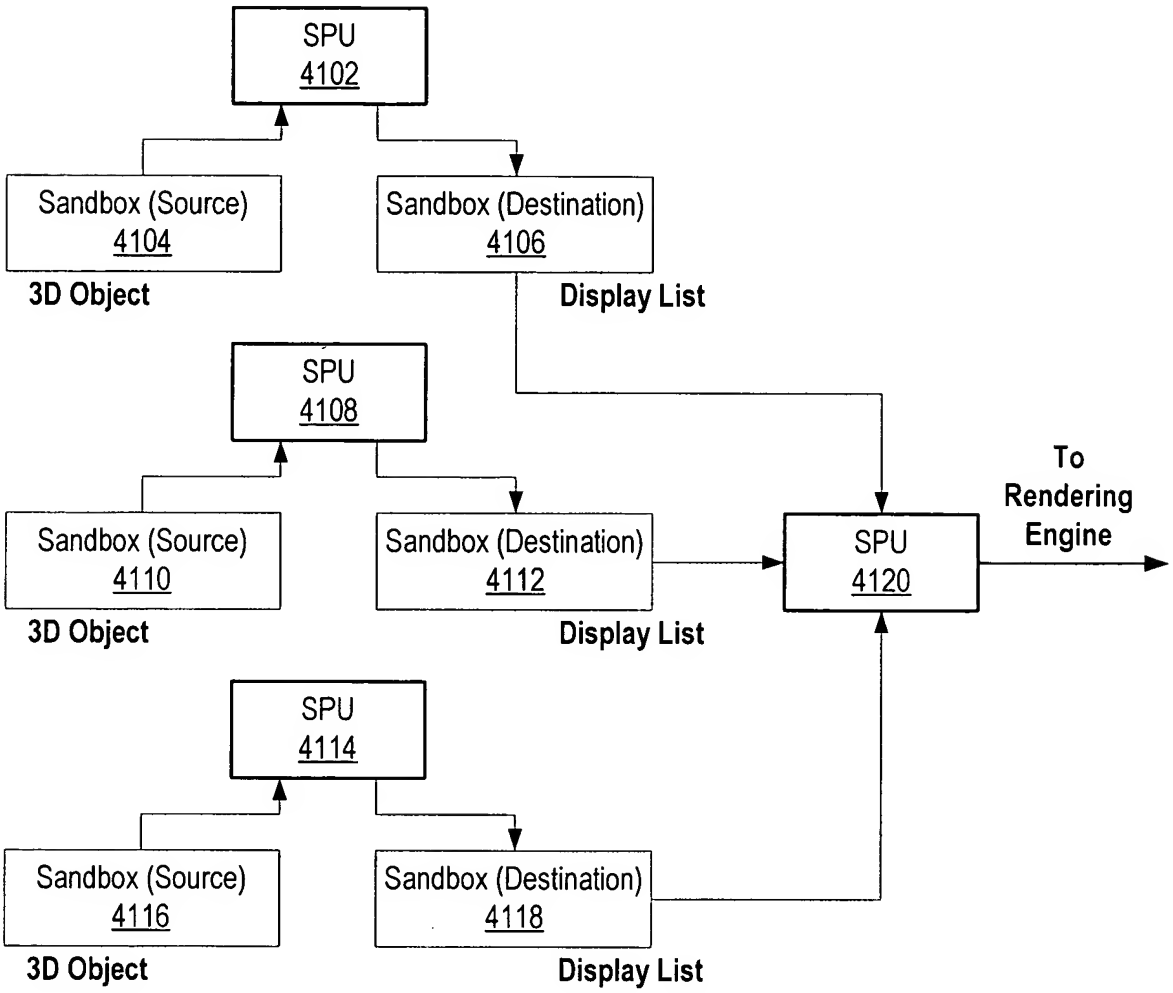
SPU
4102
Sandbox (Source)
4104
3D Object
Sandbox (Destination)
4106
Display List
SPU
4108
Sandbox (Source)
4110
3D Object
Sandbox (Destination)
4112
Display List
SPU
4120
To
Rendering
Engine
SPU
4114
Sandbox (Source)
4116
3D Object
Sandbox (Destination)
4118
Display List

Figure 41

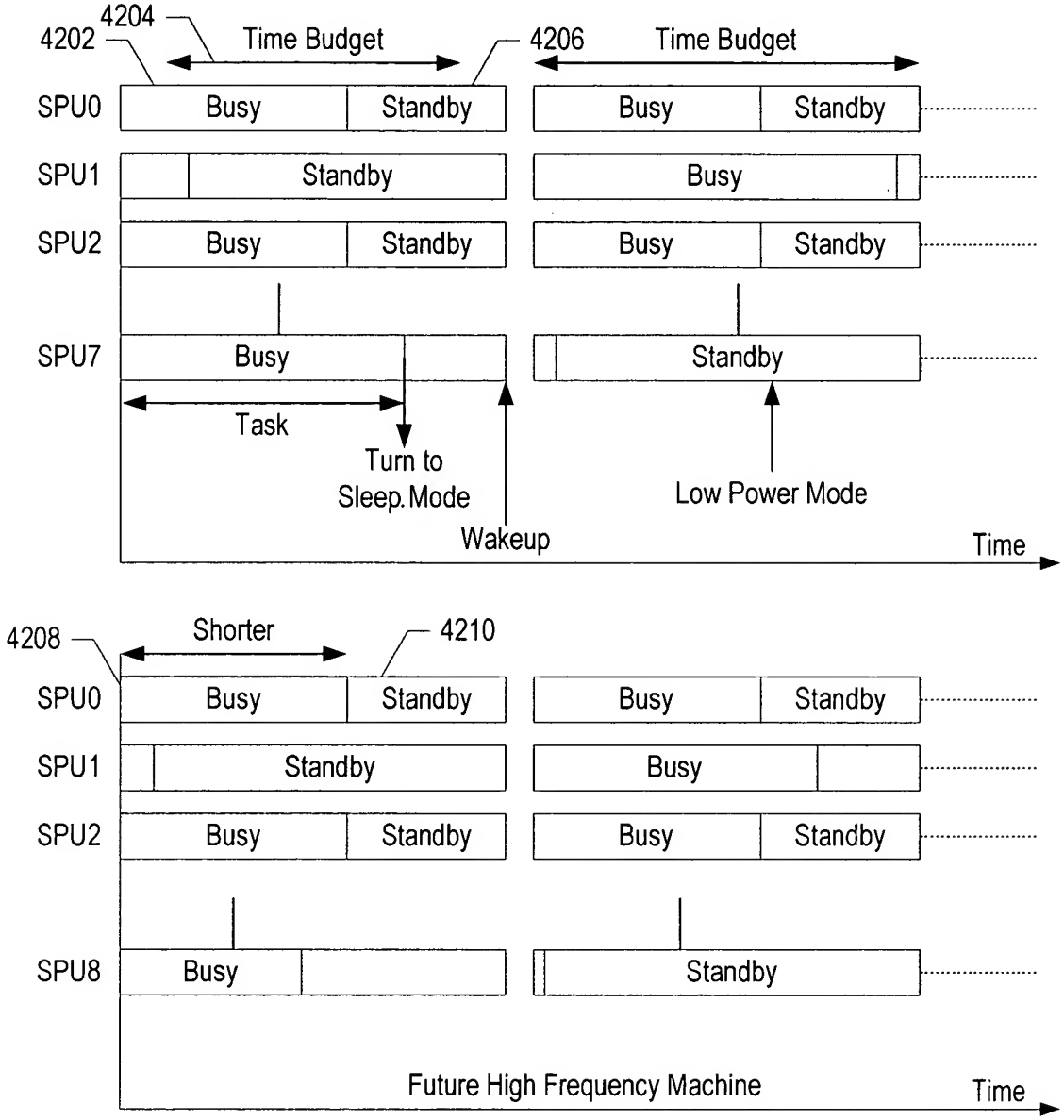
4204
4202
Time Budget
4206
Time Budget
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU7
Busy
Standby
Task
Turn to
Sleep. Mode
Low Power Mode
Wakeup
Time
4208
Shorter
4210
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU8
Busy
Standby
Future High Frequency Machine
Time

Figure 42

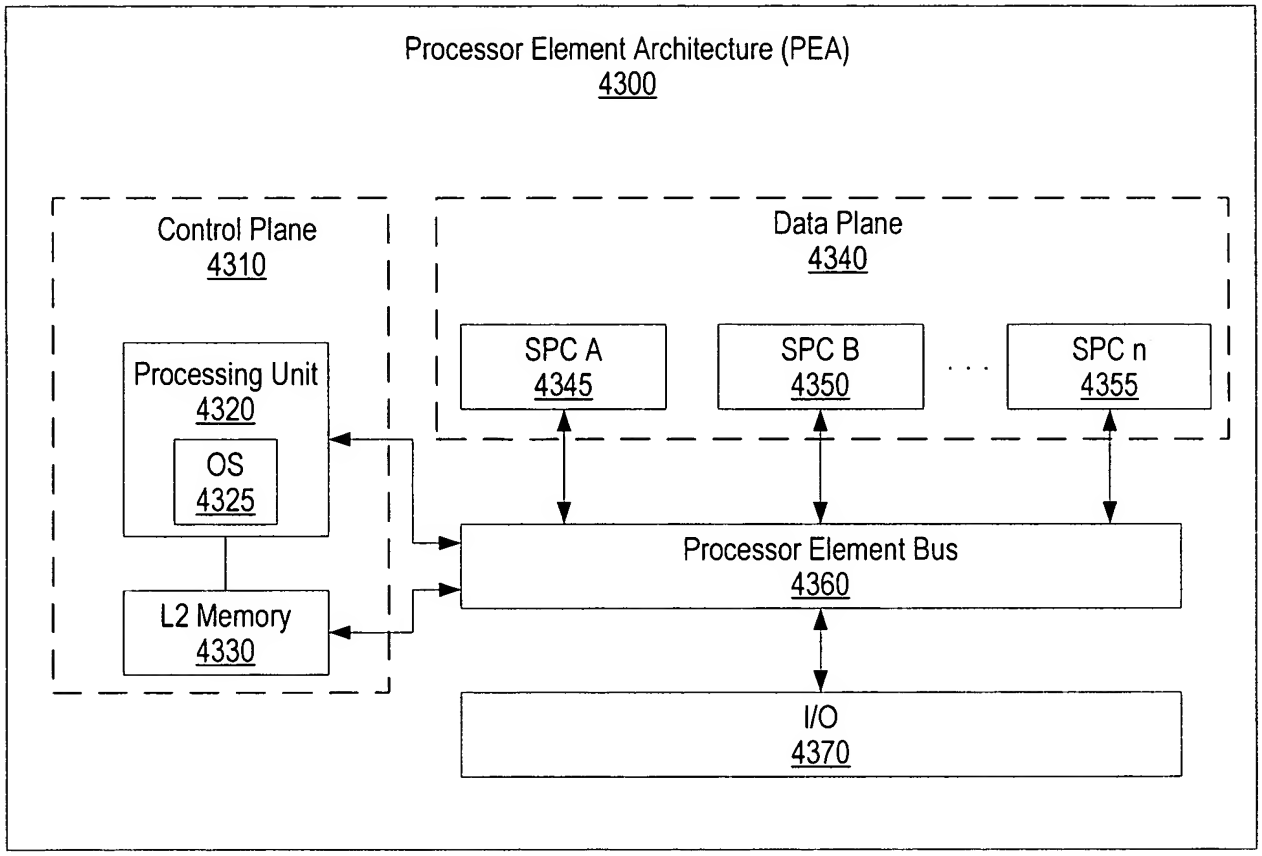
Processor Element Architecture (PEA)
4300
Control Plane
4310
Processing Unit
4320
OS
4325
L2 Memory
4330
Data Plane
4340
SPC A
4345
SPC B
4350
SPC n
4355
Processor Element Bus
4360
I/O
4370

Figure 43

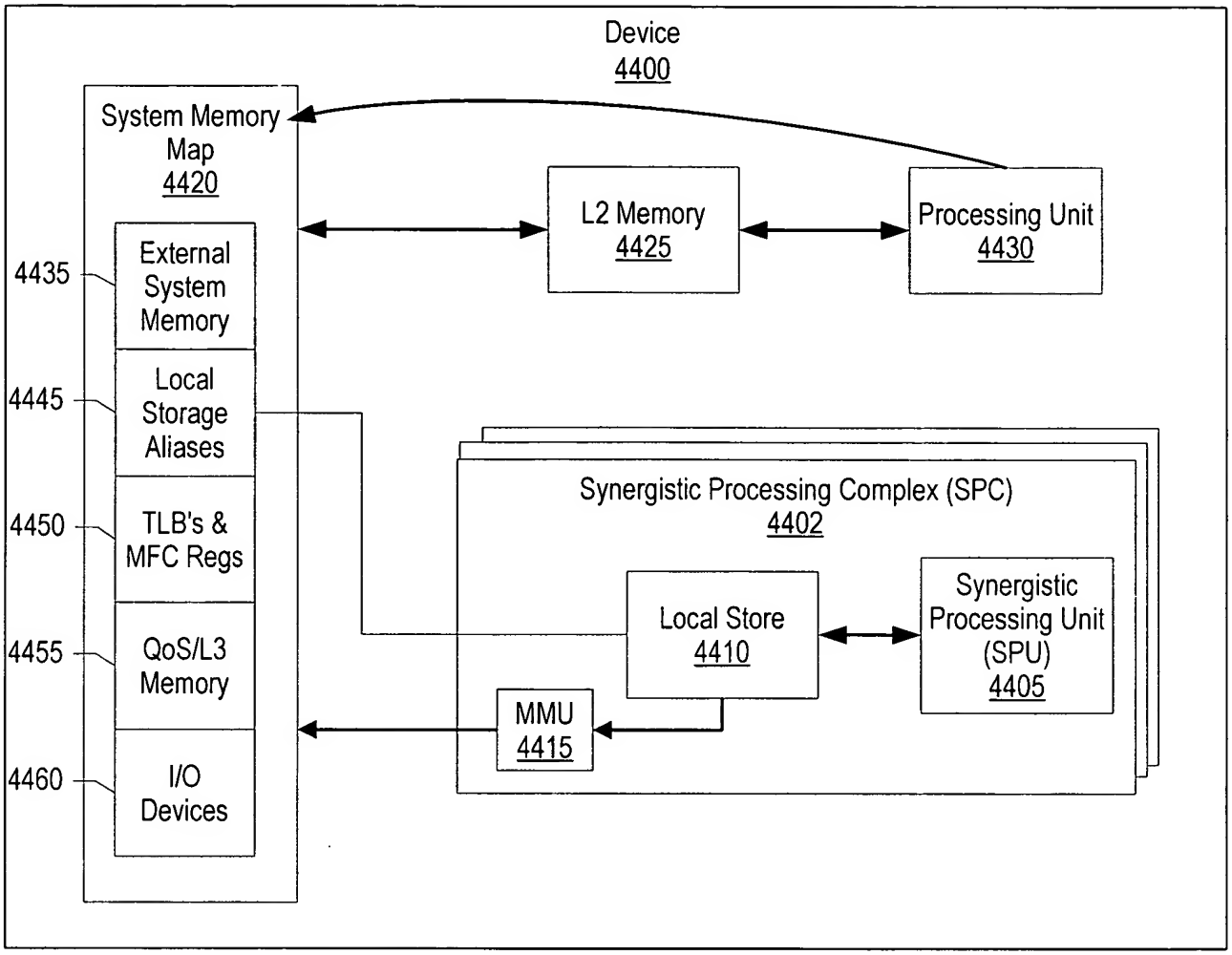

Figure 44A

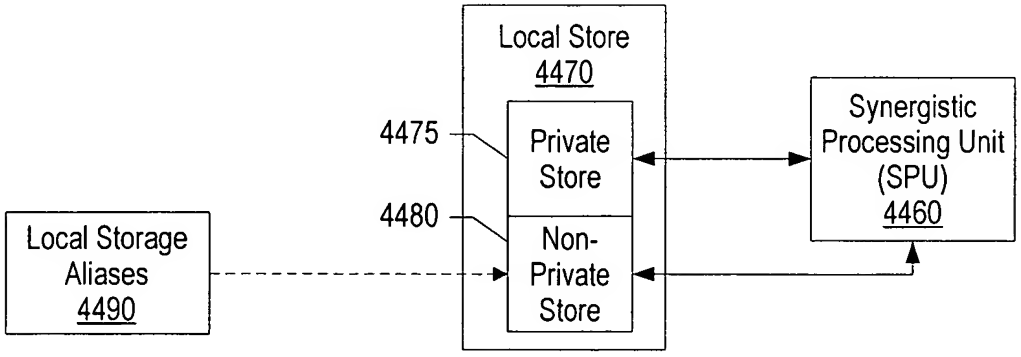

Figure 44B

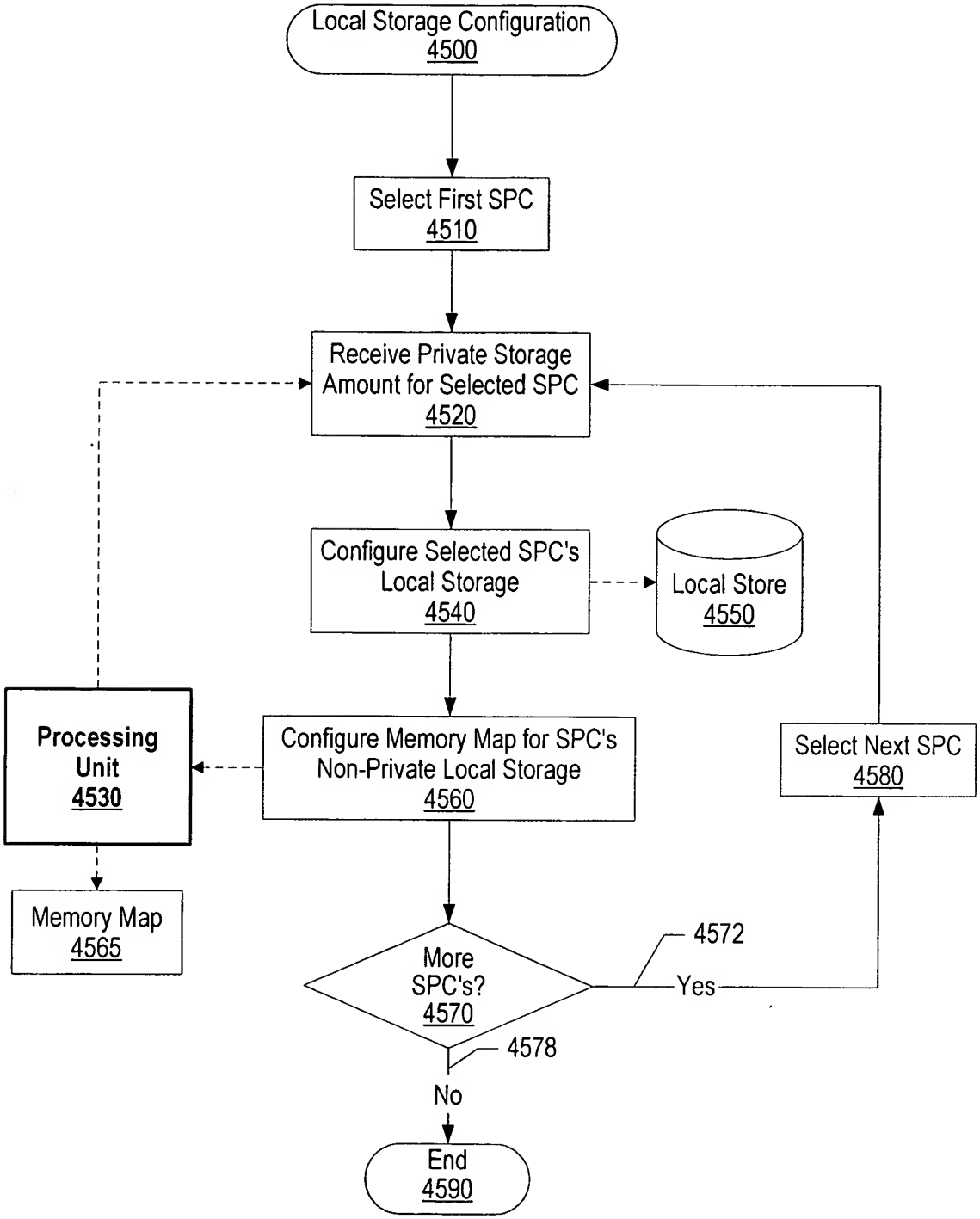
Local Storage Configuration
4500
Select First SPC
4510
Receive Private Storage Amount for Selected SPC
4520
Configure Selected SPC's Local Storage
4540
Local Store
4550
Processing Unit
4530
Configure Memory Map for SPC's Non-Private Local Storage
4560
Select Next SPC
4580
Memory Map
4565
More SPC's?
4570
4572
Yes
4578
No
End
4590

Figure 45

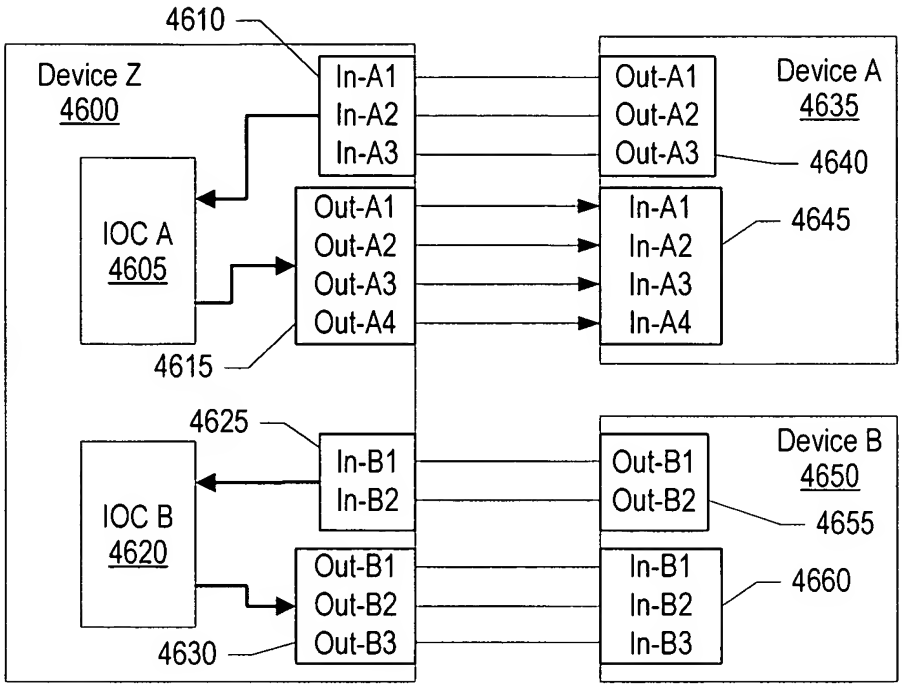

Figure 46A (Prior Art)

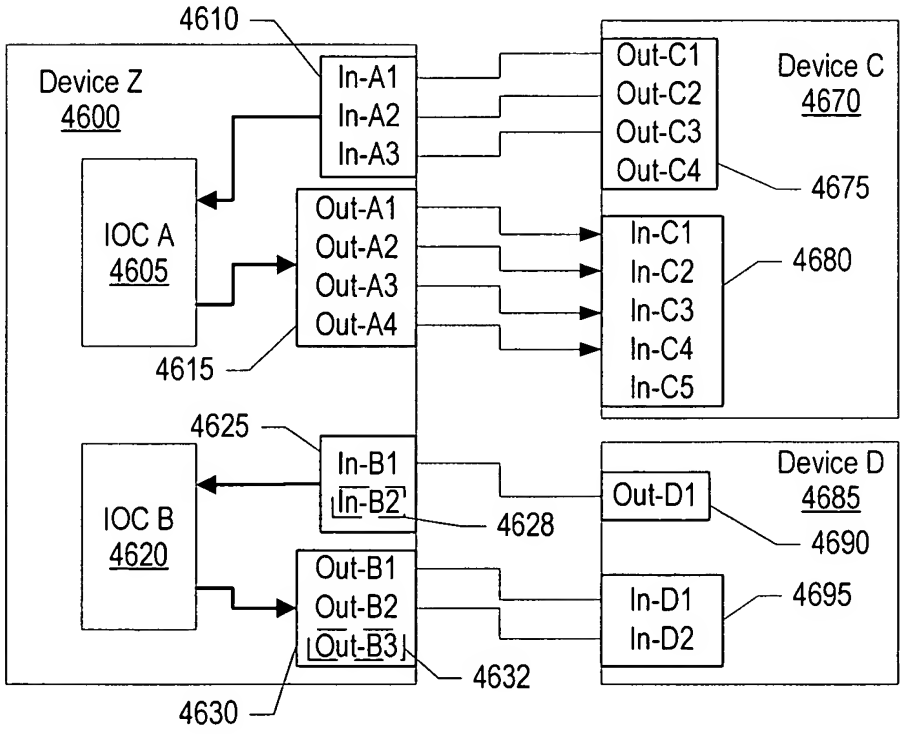

Figure 46B (Prior Art)

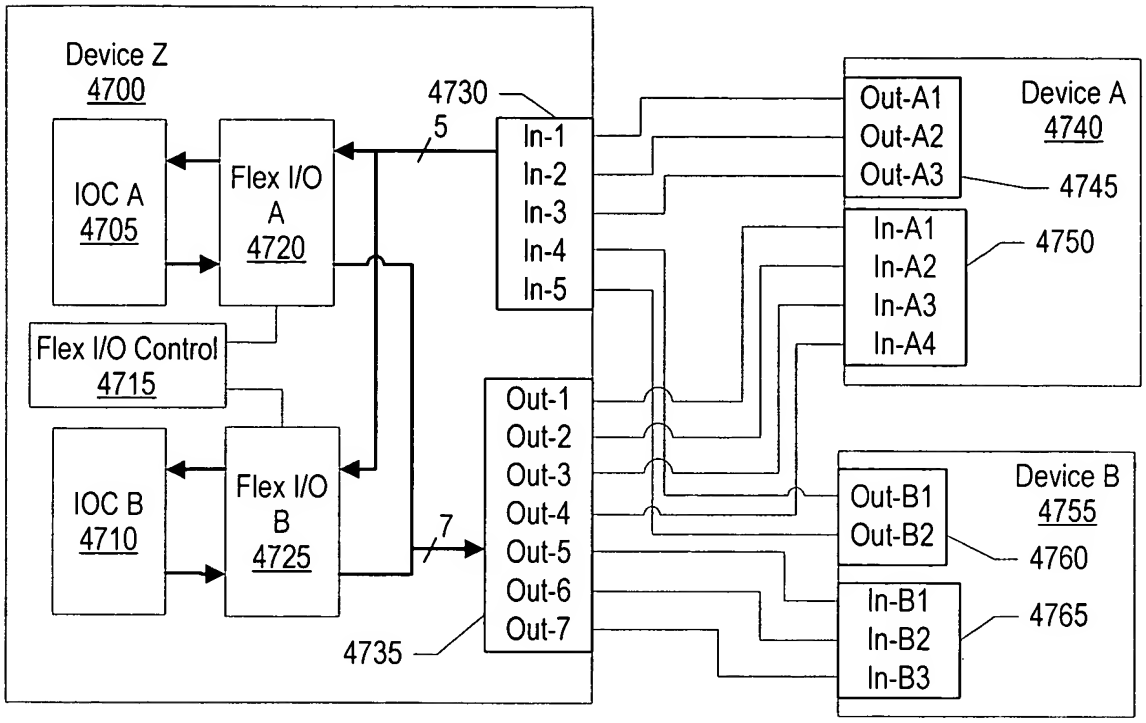

Figure 47A

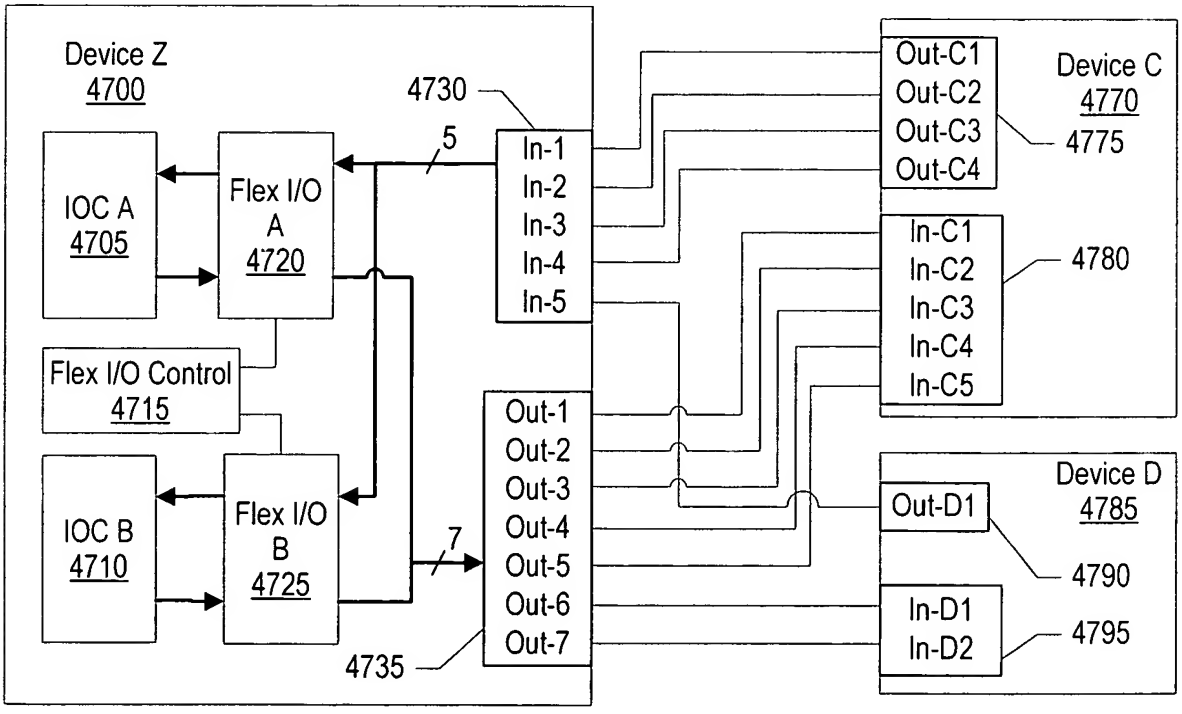

Figure 47B

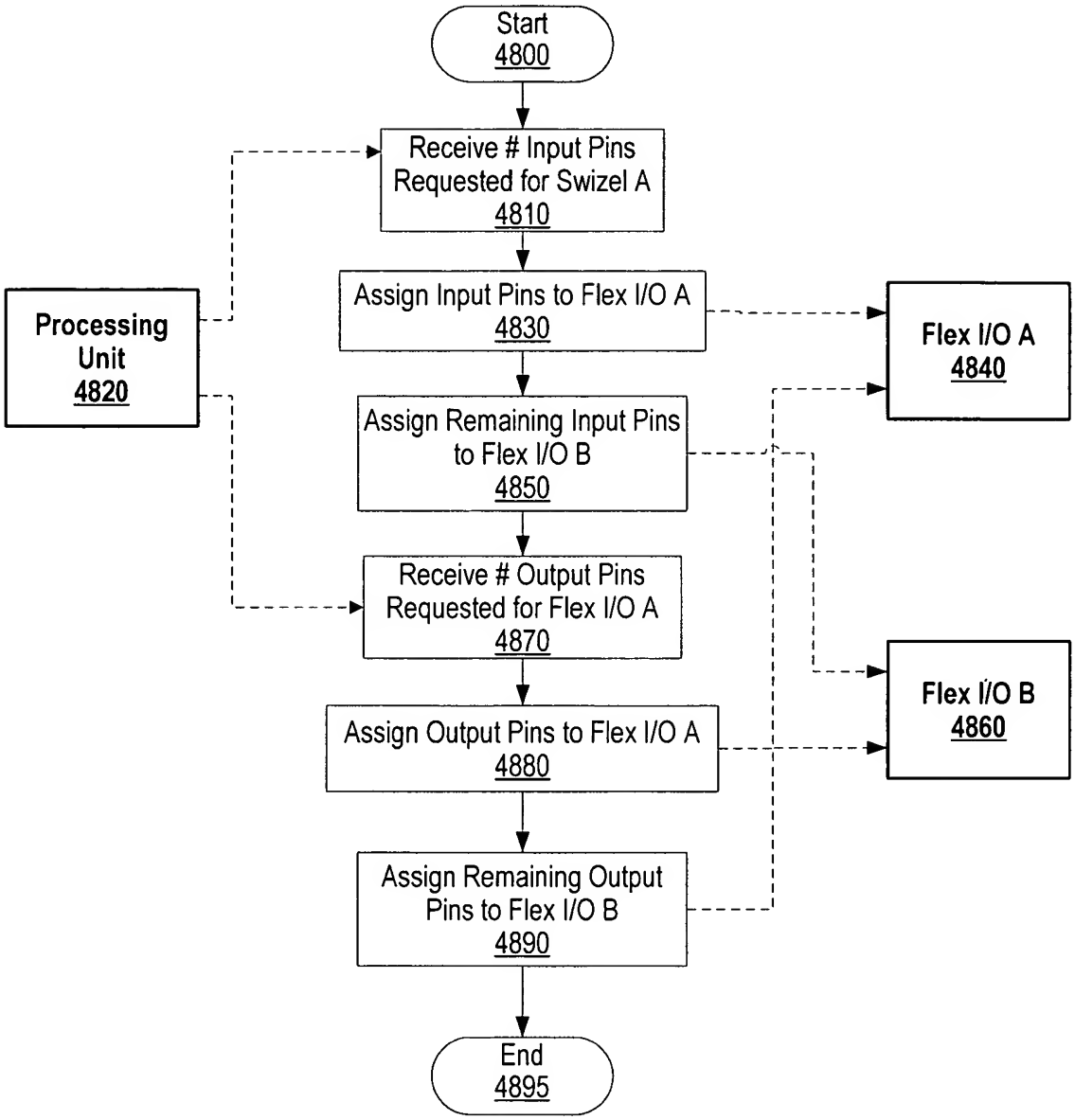
Start
4800
Receive # Input Pins Requested for Swizel A
4810
Assign Input Pins to Flex I/O A
4830
Processing Unit
4820
Flex I/O A
4840
Assign Remaining Input Pins to Flex I/O B
4850
Receive # Output Pins Requested for Flex I/O A
4870
Flex I/O B
4860
Assign Output Pins to Flex I/O A
4880
Assign Remaining Output Pins to Flex I/O B
4890
End
4895

Figure 48

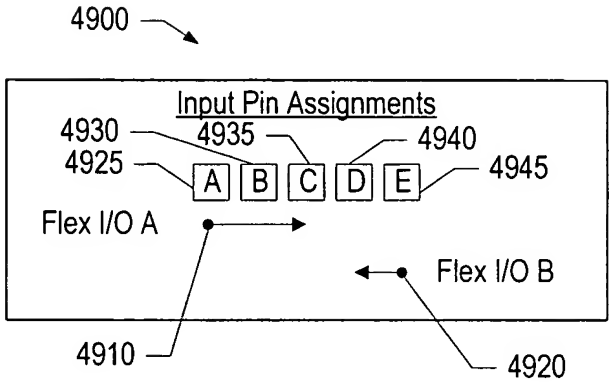

Figure 49A

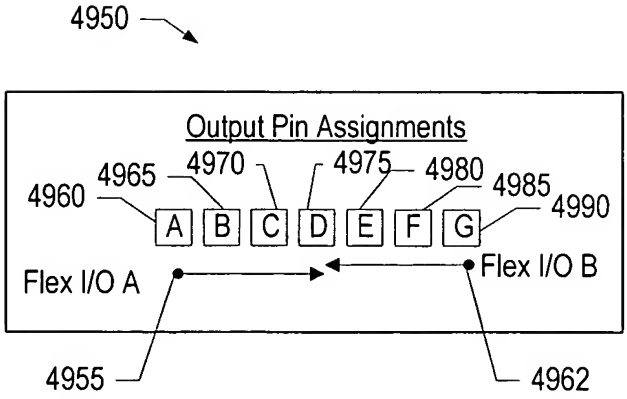

Figure 49B

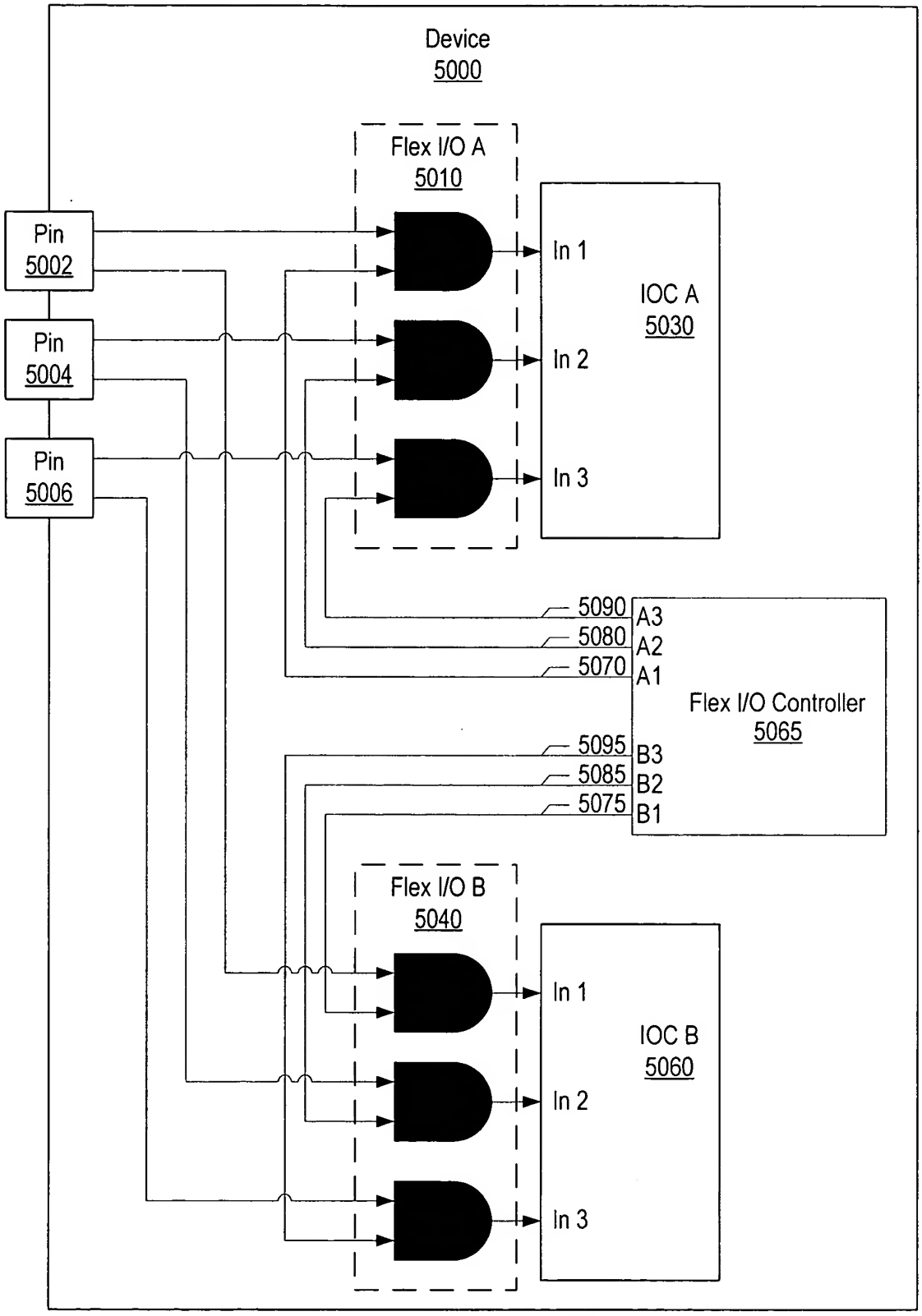
Device
5000
Flex I/O A
5010
Pin
5002
Pin
5004
Pin
5006
In 1
In 2
In 3
IOC A
5030
5090
5080
5070
A3
A2
A1
Flex I/O Controller
5065
5095
5085
5075
B3
B2
B1
Flex I/O B
5040
In 1
In 2
In 3
IOC B
5060

Figure 50